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MS-7A94

Basinfall Platform

ATX

Ver: 20

CPU:

System Chipset:

Skylake X/Kabylake X

Kaby Lake PCH-X

Onboard Chip:

HD Audio Codec:ALC1220

LAN-Intel i219

SIO:NTC6795D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

DDRIV (UP to 2677MHz) * 8DIMM (4 Channel)

ACPI:

MPS

PWM:

VR13 -IR35201

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X8) Slot * 1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 1

Other:

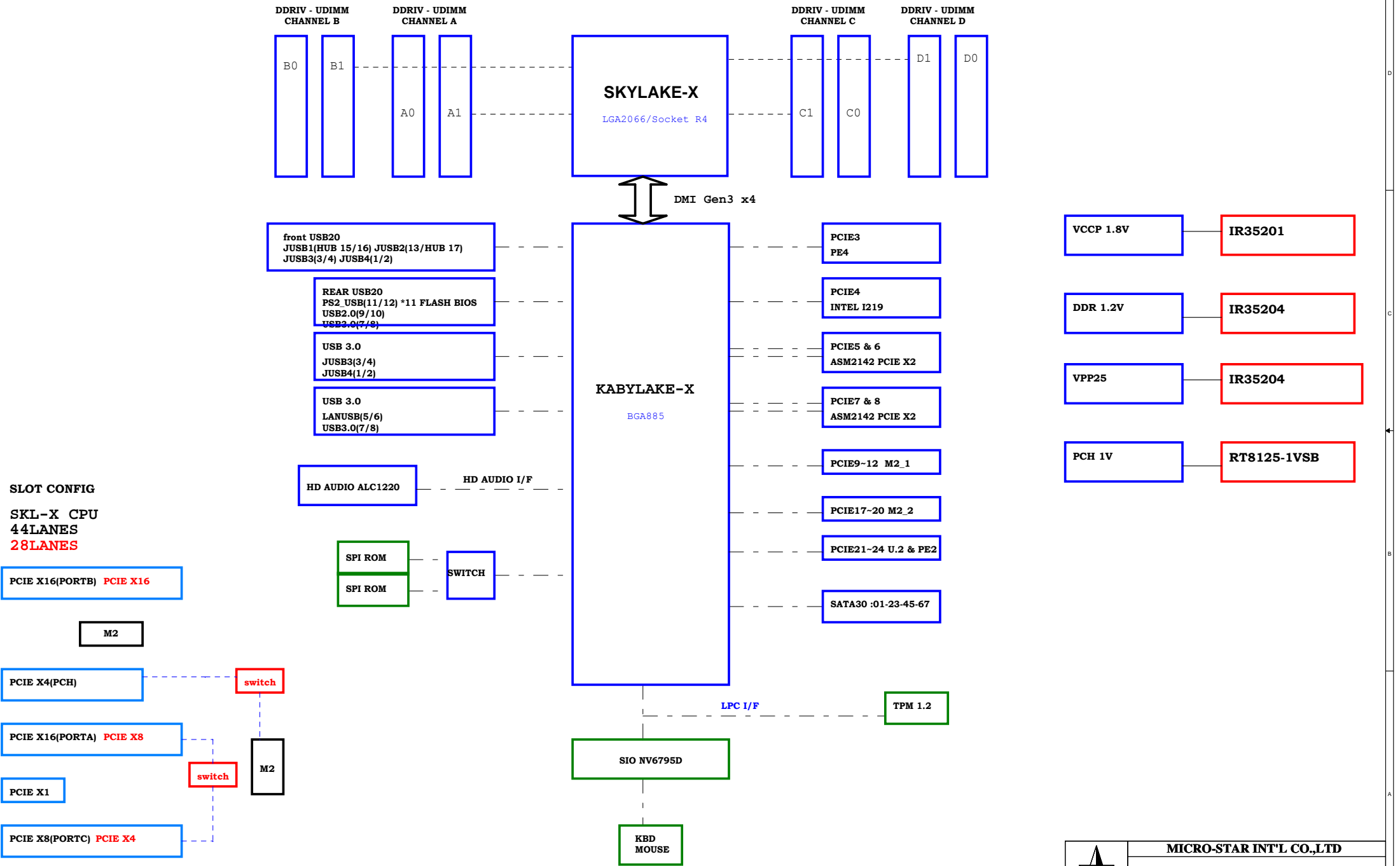
SATA3.0 *8

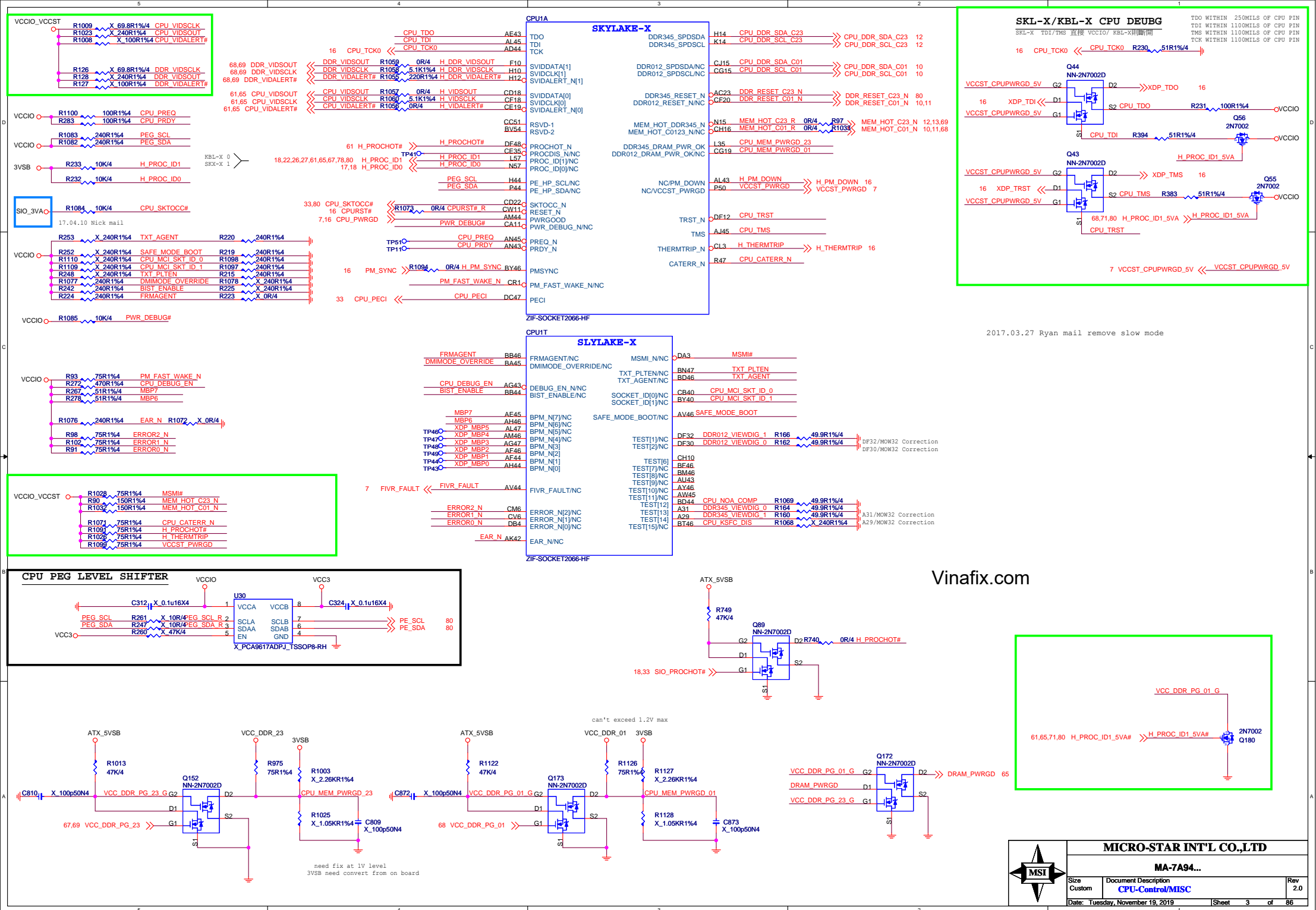
USB2.0 *6 Ports (4R/4F)

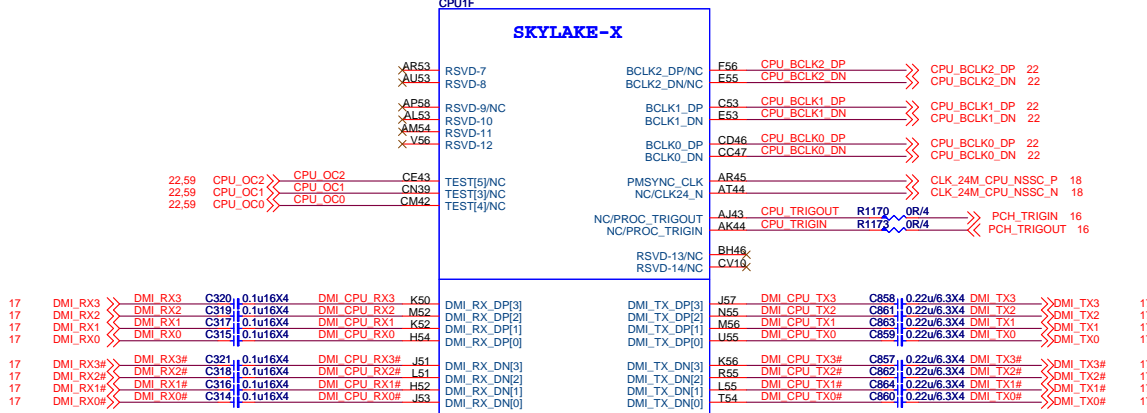
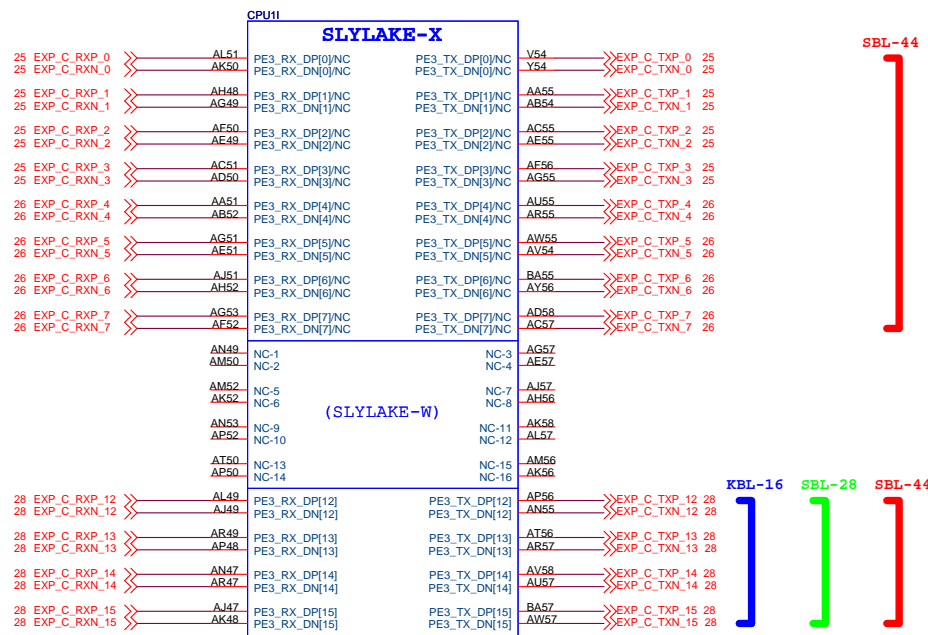
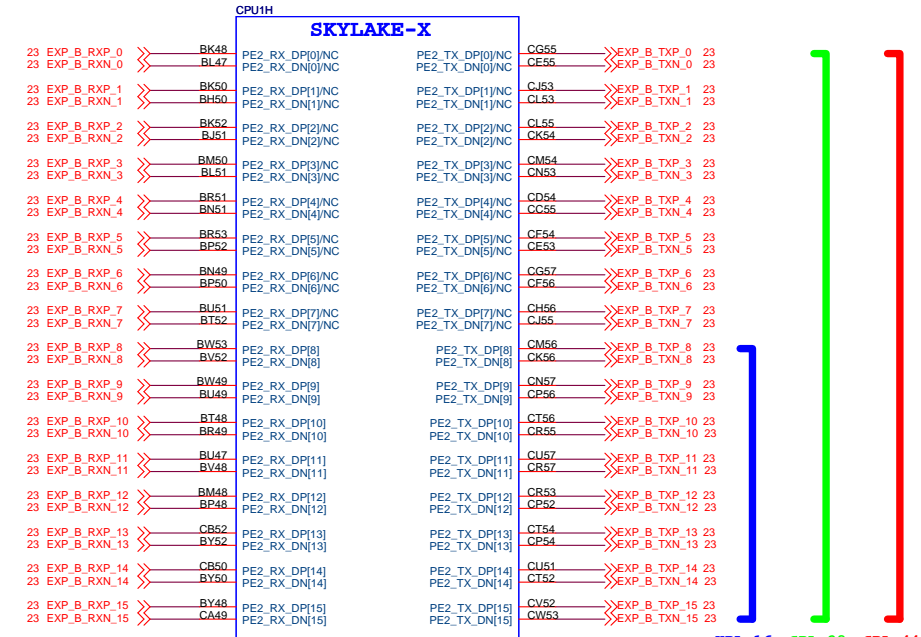
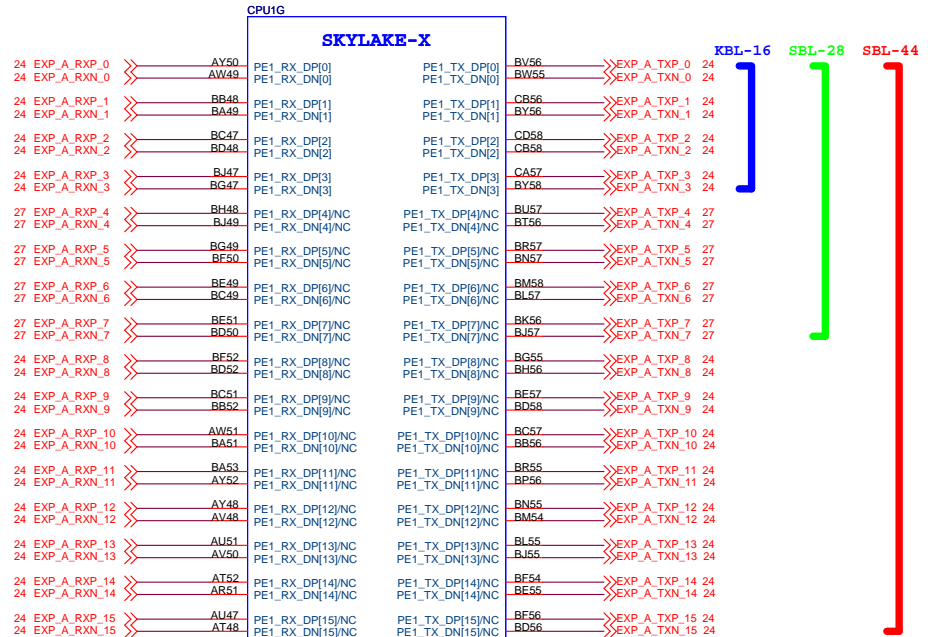
REAR USB30*4 + USB3.1*1 & TYPEC*1

FRONT USB3.0 *4+TYPEC*1

MS-7A94 Block Diagram








VCCIO R1104 510R/4 CPU_OC2 R1103 X 10K/4
VCCIO R1105 510R/4 CPU_OC1 R1092 X 10K/4
VCCIO R1106 510R/4 CPU_OC0 R1093 X 10K/4

CPU_OC[2:0]	BCLK (MHZ)	PCIE RATIO
1 1 1	100	10
1 1 0	111	9
1 0 1	125	8
1 0 0	142.5	7
0 1 1	167	6
0 1 0	200	5
0 0 1	250	4

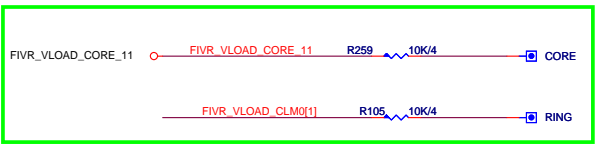
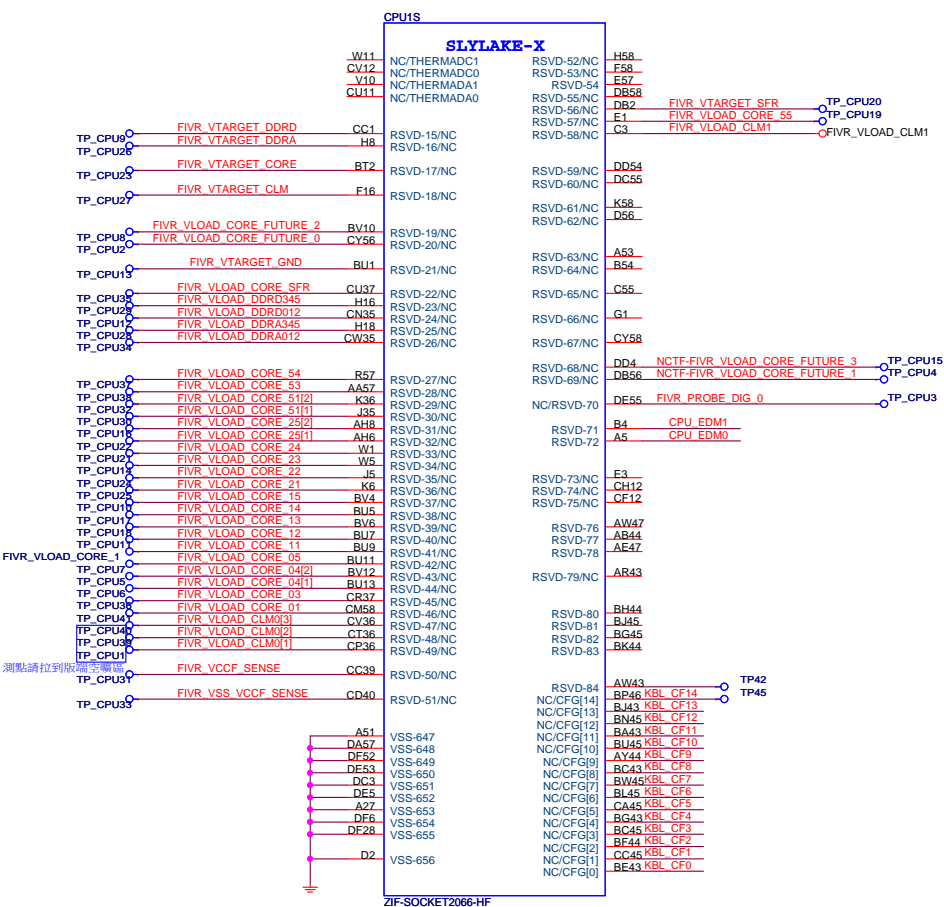
COLD RESET

 **MICRO-STAR INT'L CO.,LTD**

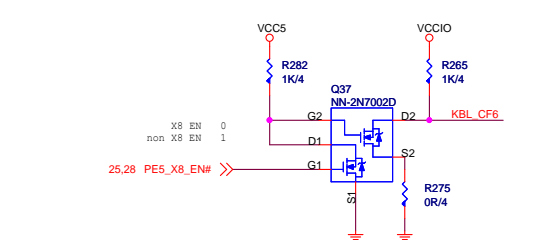
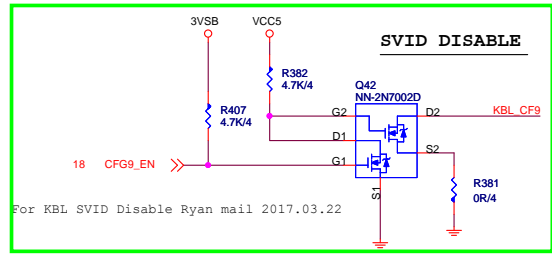
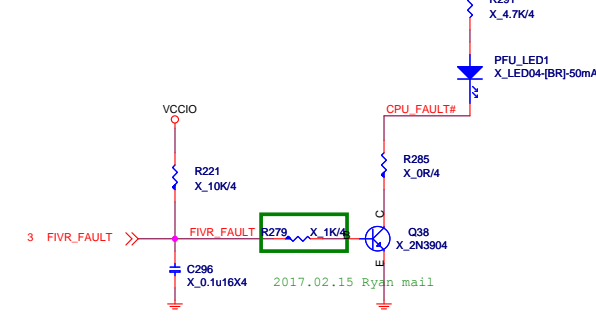
MA-7A94...

Size	Document Description	Rev
Custom	CPU-PEG/DMI	2.0

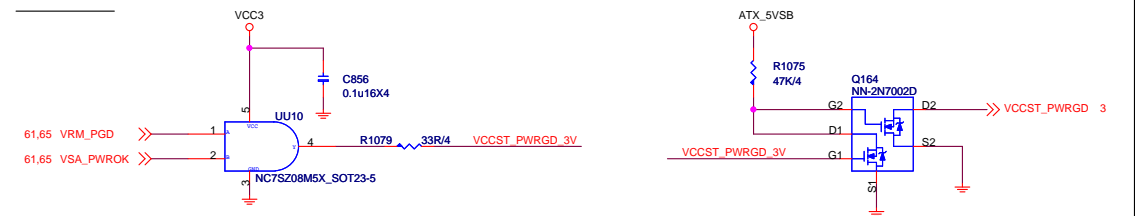
Date: Tuesday, November 19, 2019 | Sheet 6 of 86



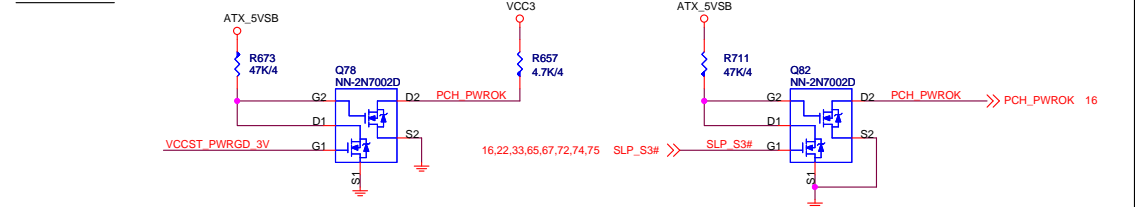
POWER FAULT LED



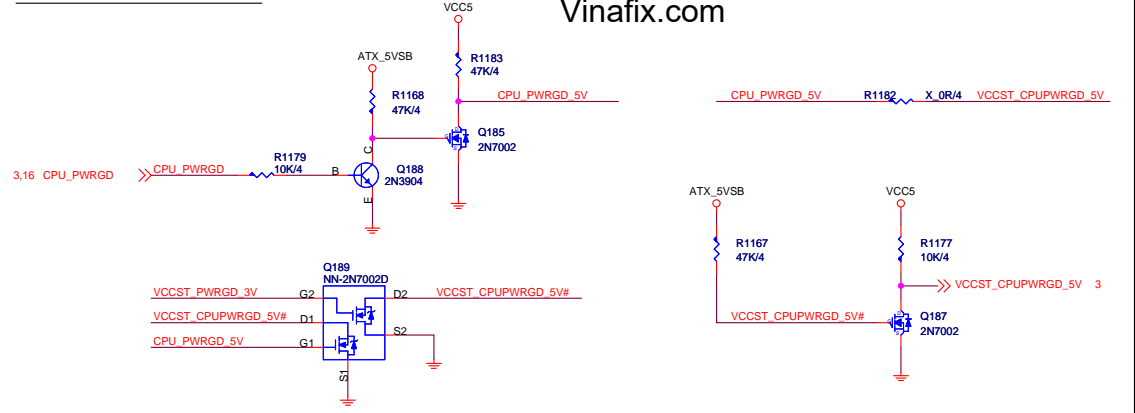
VCCST_PWRGD



PCH_PWROK



SKL-X/KBL-X CPU DEUBG

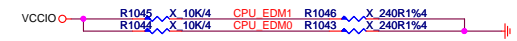


PCIE Strap

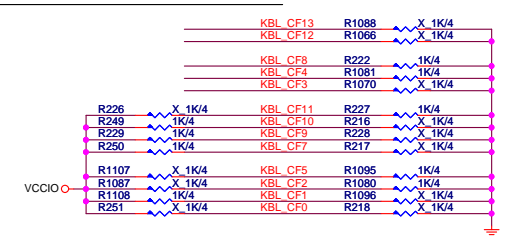
CFG6	CFG5	PCIE
0	0	1x8,2x4
0	1	RSVD
1	0	2x8
1	1	1x16

CFG Strap

CFG Table		
HIGH	LOW	DESCRIPTION
0	No Lock	Lock
1	No Lock	Lock
2	NORM	REVERSE
3		PEG LANE REVERSAL
4	DISABLE	ENABLE
5	DISABLE	ENABLE
6	DISABLE	ENABLE
7	RESET#	BTOS REQ
8	RSVD	PEG DEFER TRAINING
9	PRESENT	NO PRESENT
10		SVID PRESENT
11		RSVD
12		RSVD
13		RSVD
14	RSVD	
15	RSVD	



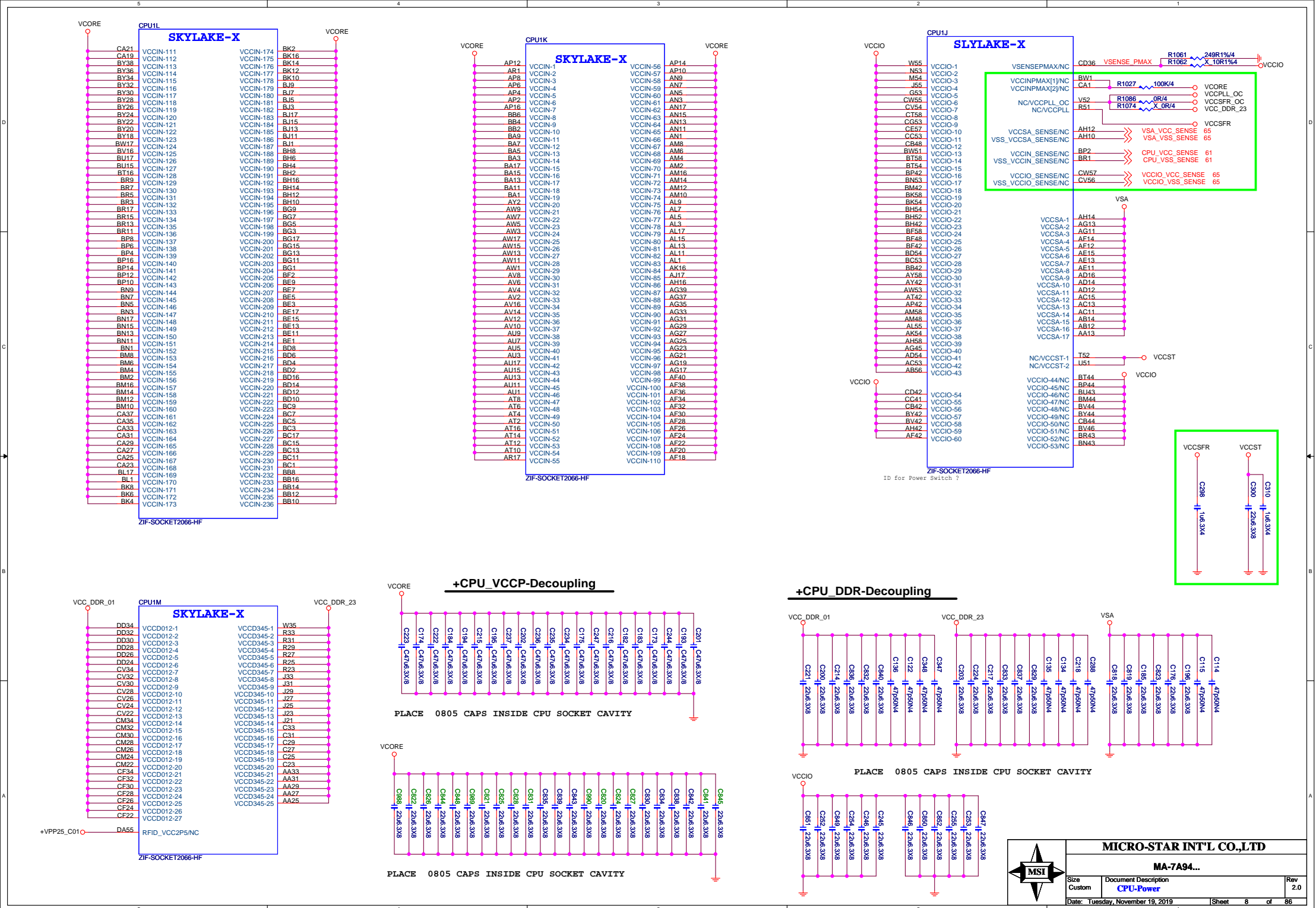
CPU KBLX STRAP SIGNALS

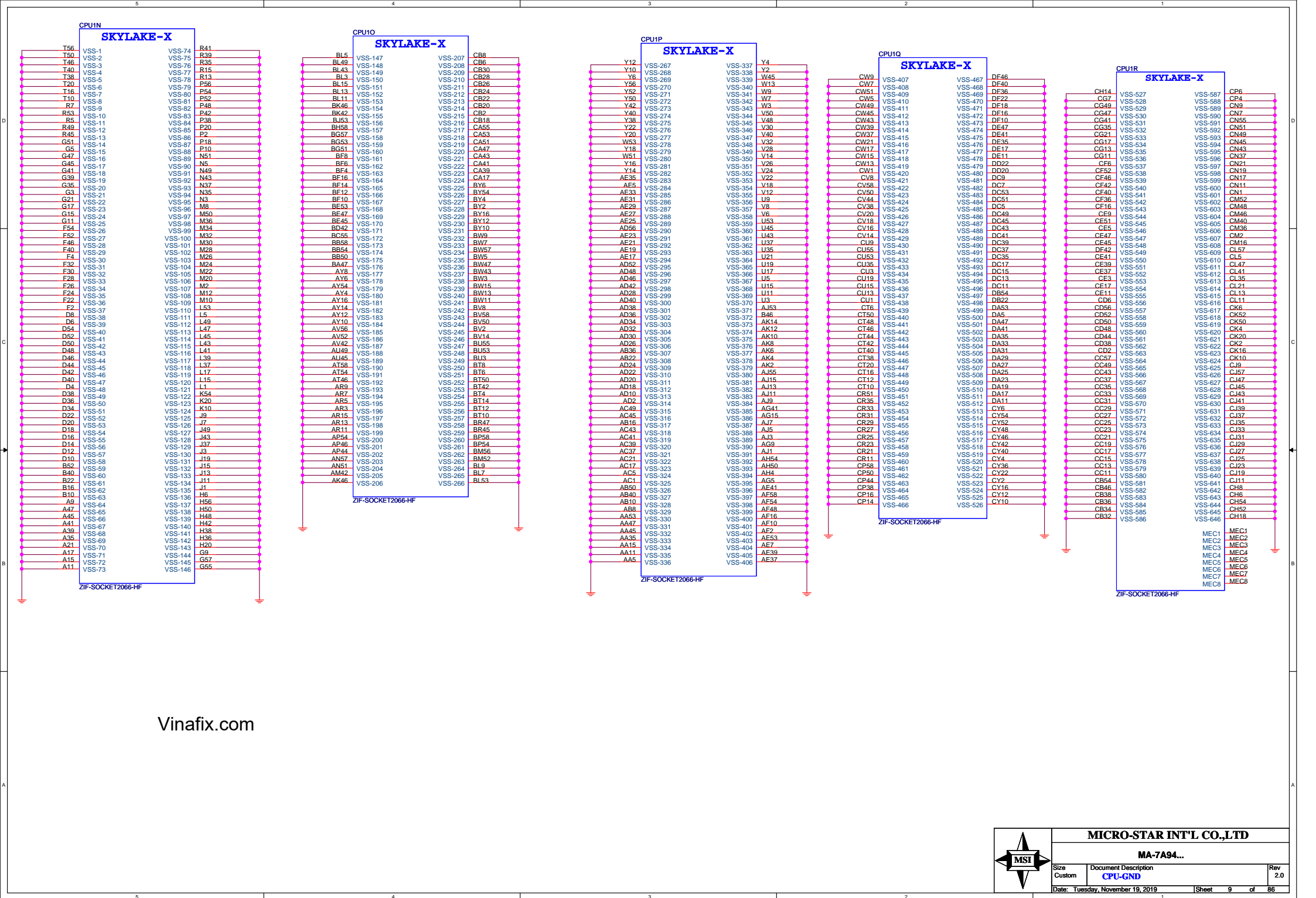


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MA-7A94...

Size	Document Description	Rev
Custom	CU-PSVD	2.0
Date:	Tuesday, November 19, 2019	Sheet 7 of 86



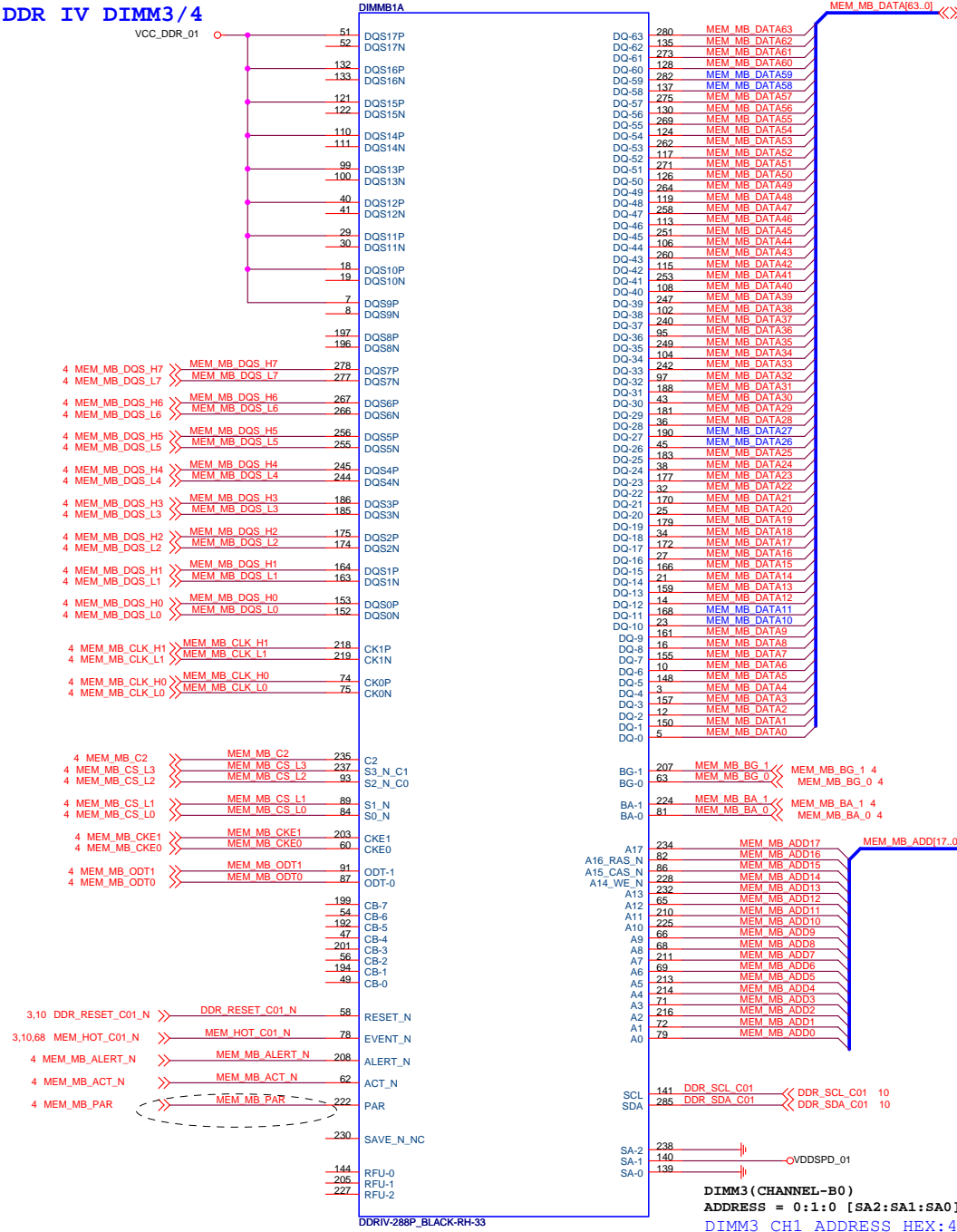


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2017.02.13 Ryan mail
DQS9~17P PU to VCC



DDR IV DIMM3/4



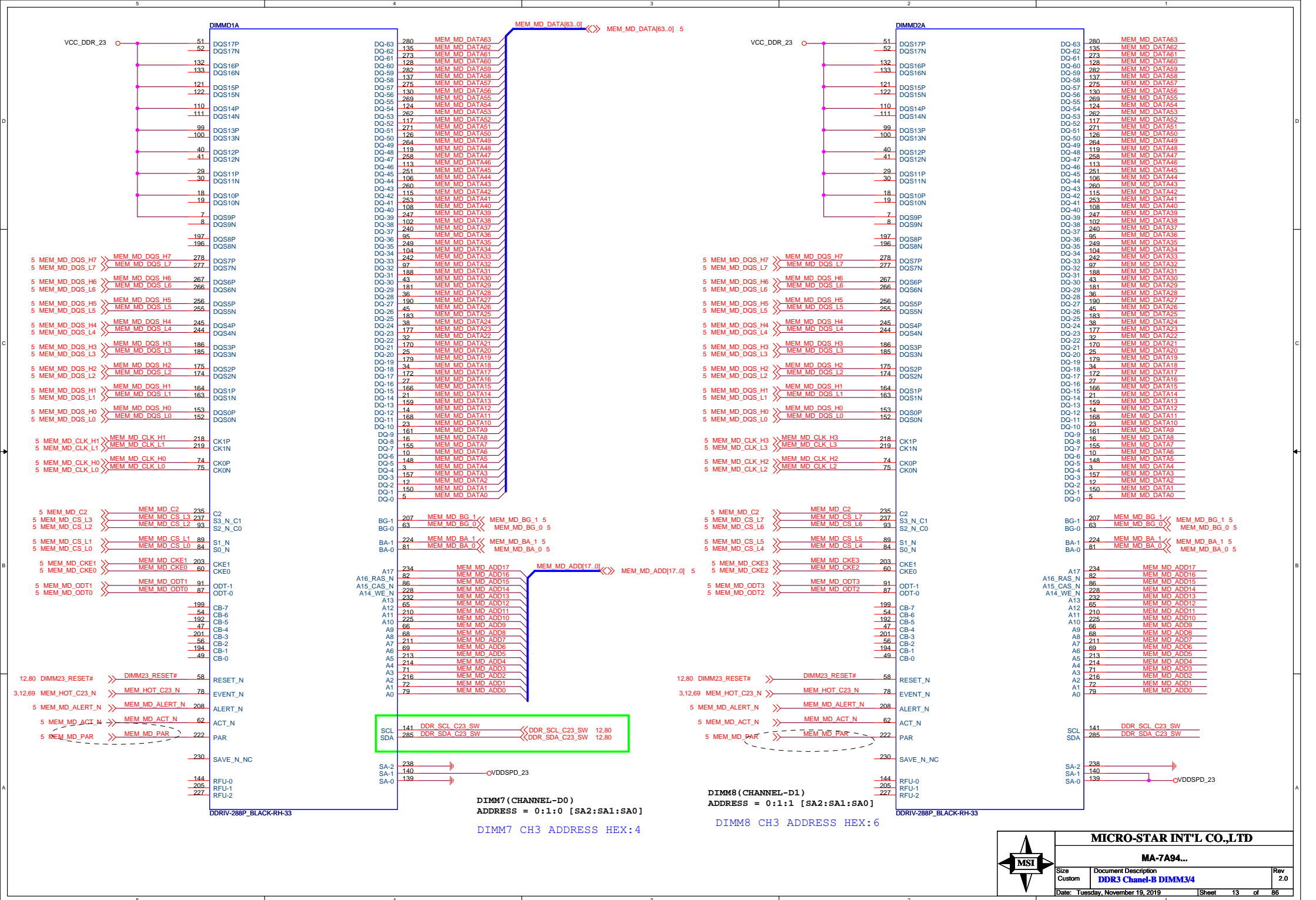
DIMM4 (CHANNEL-B1)
ADDRESS = 0:1:1 [SA2:SA1:SA0]
DIMM4 CH1 ADDRESS HEX:6



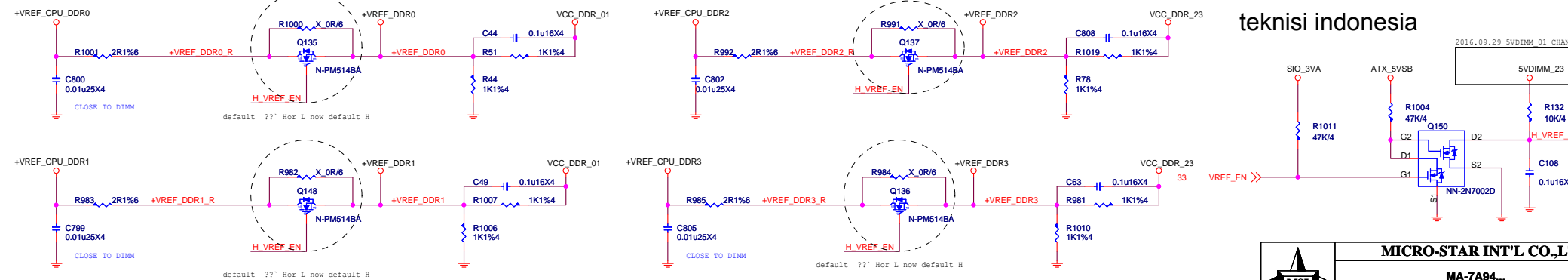
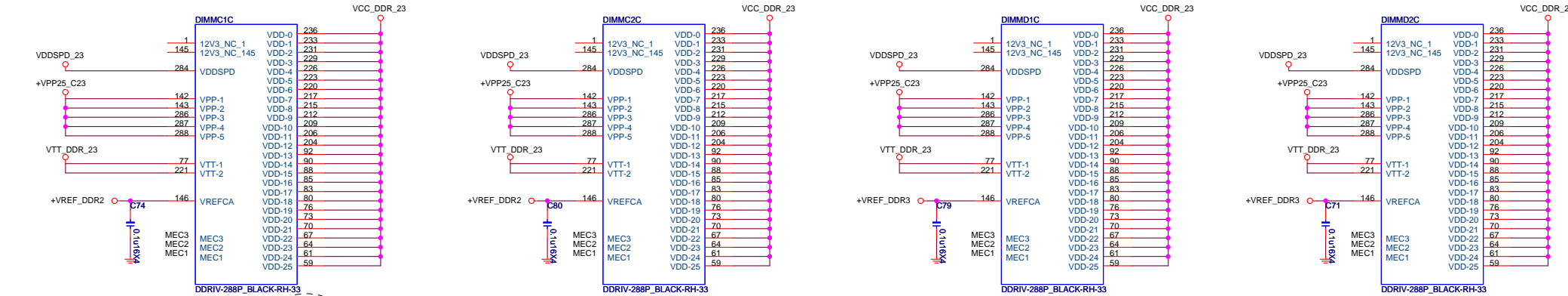
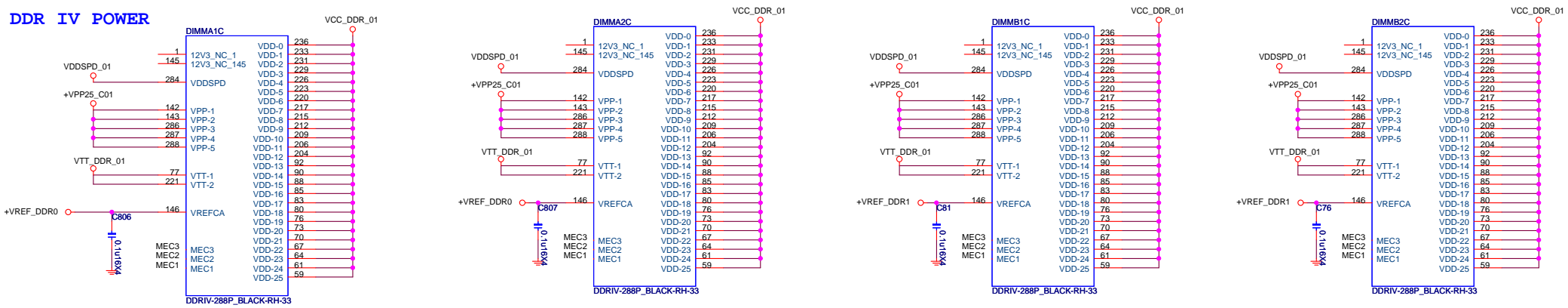
MICRO-STAR INT'L CO.,LTD

MA-7A94...

Size	Document Description	Rev
Custom	DDR IV DIMM3/4	2.0
Date:	Tuesday, November 19, 2019	Sheet 11 of 86

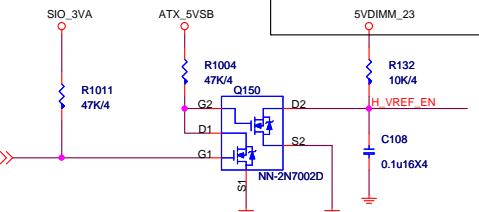


DDR IV POWER



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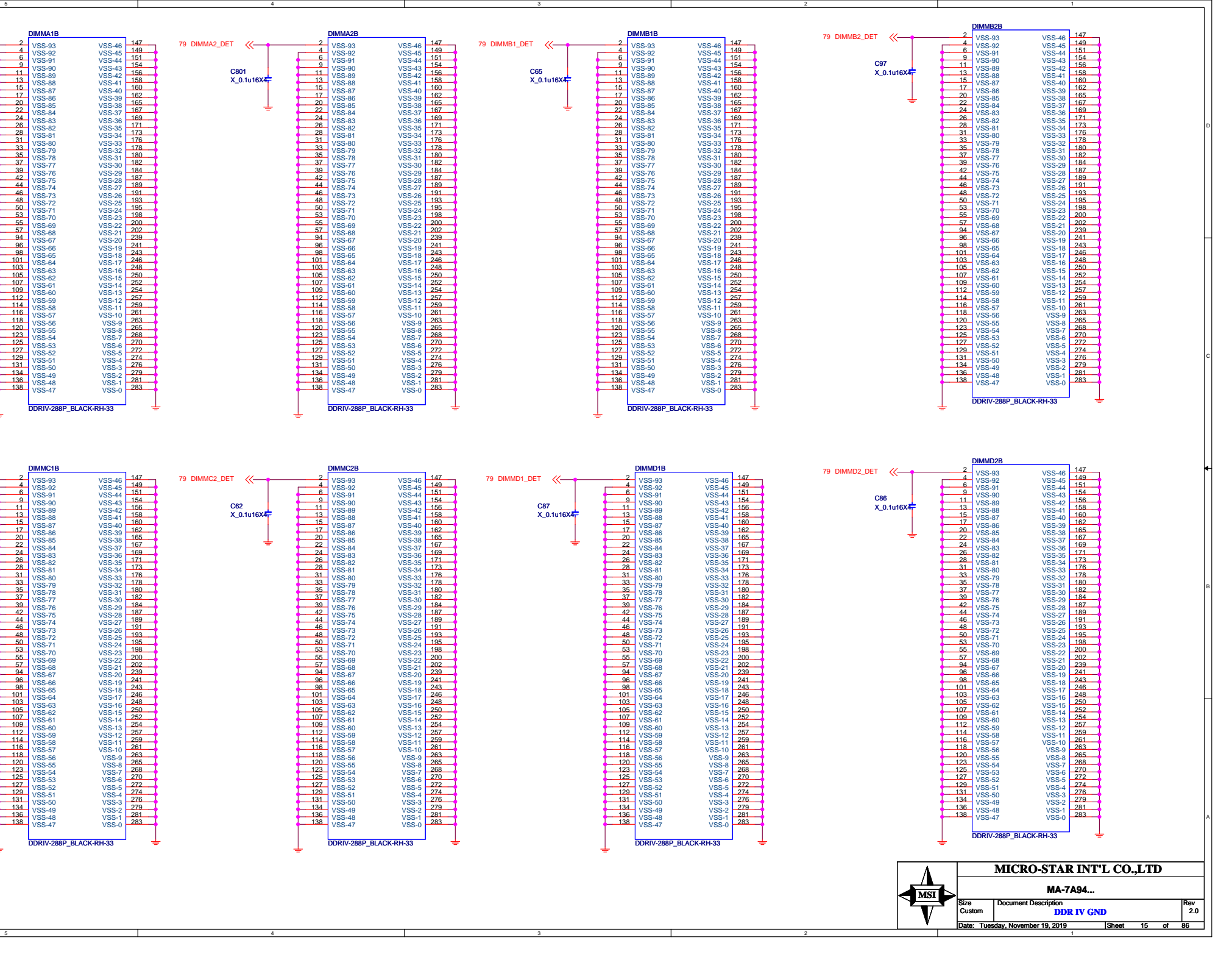
2016.09.29 5VDIMM 01 CHANGE TO 5VDIMM 23



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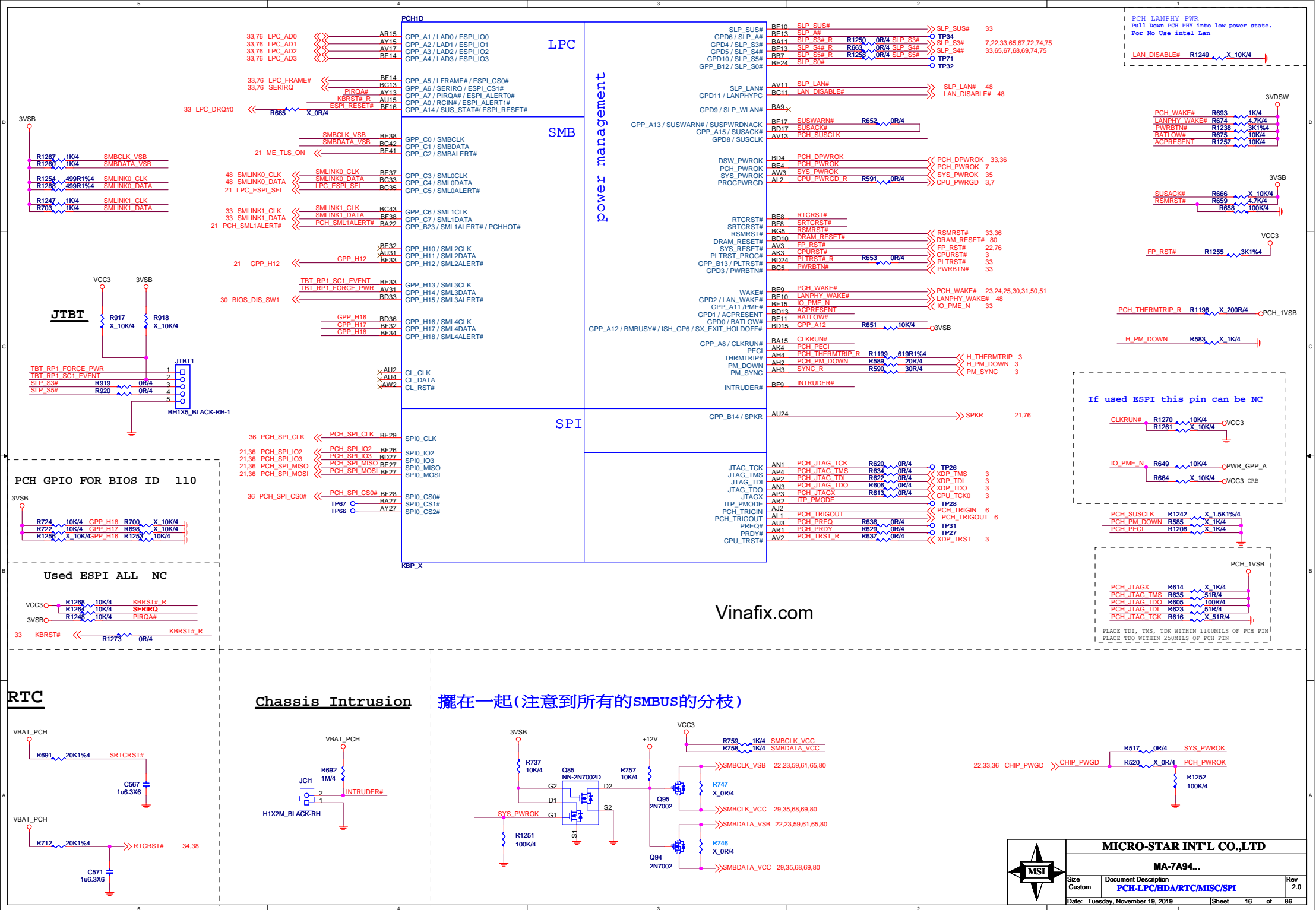
MA-7A94...

Size Custom	Document Description DDR IV POWER	Rev 2.0
Date: Tuesday, November 19, 2019		Sheet 14 of 86

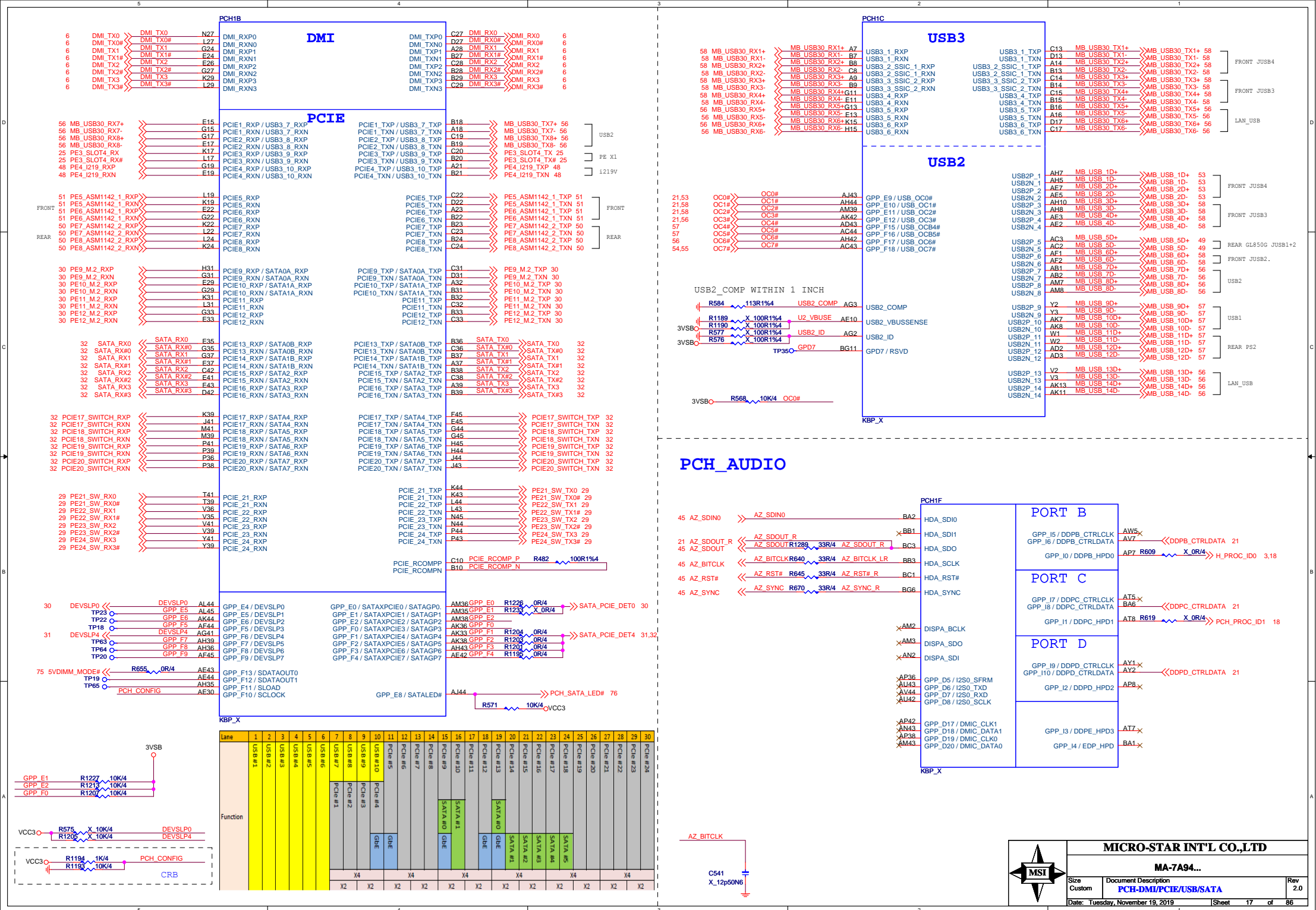
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MA-7A94...

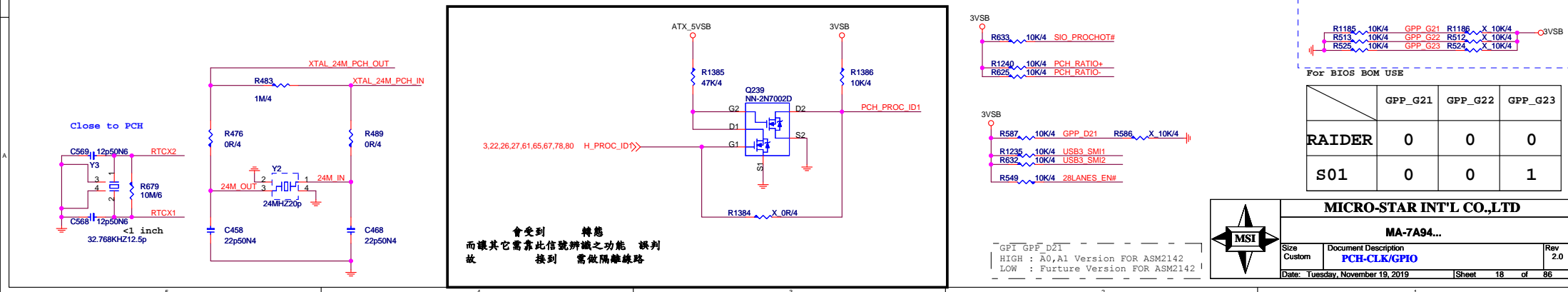
Date: Tuesday, November 19, 2019	Sheet 15 of 86
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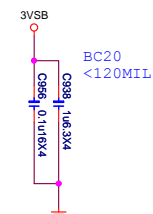
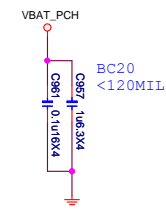
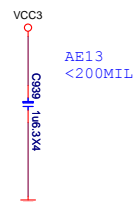
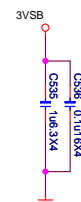
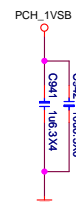
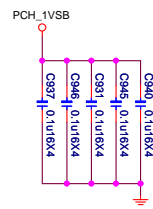
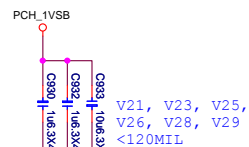
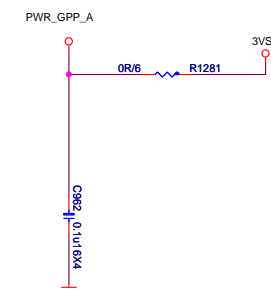
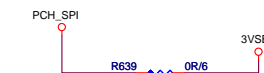
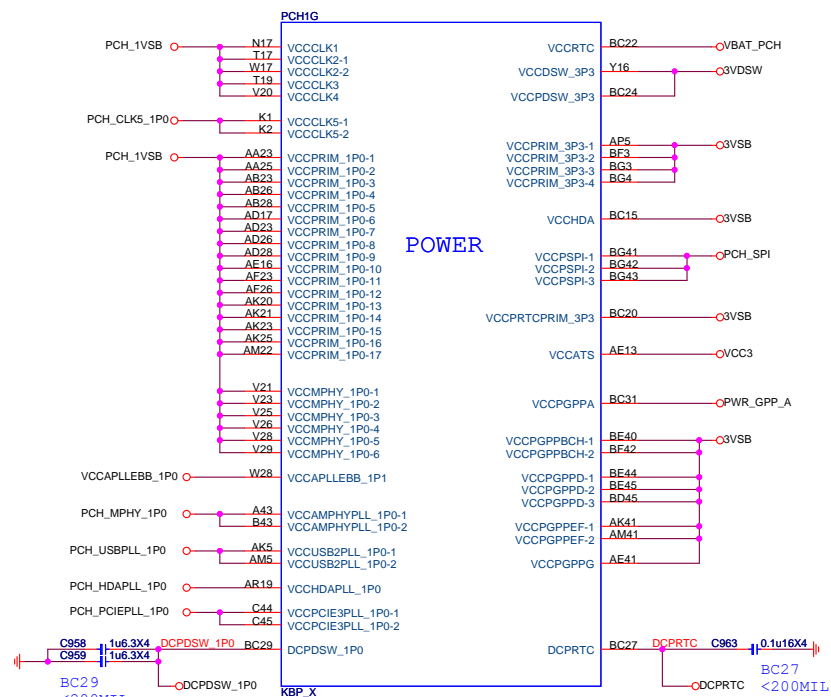
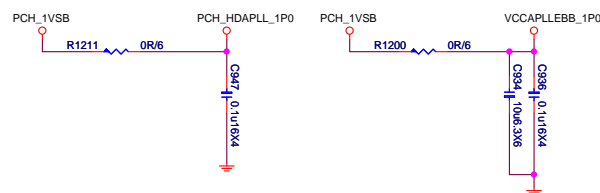
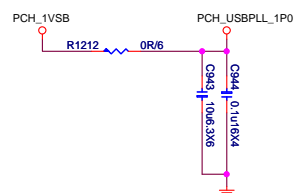
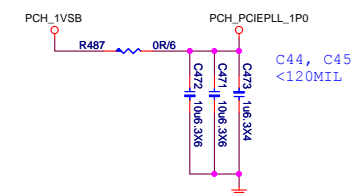
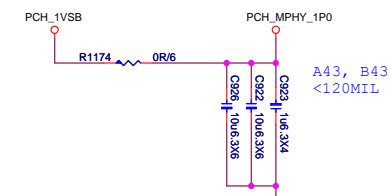
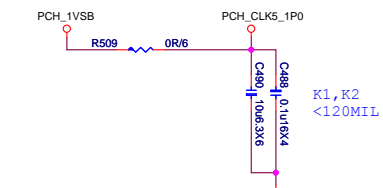


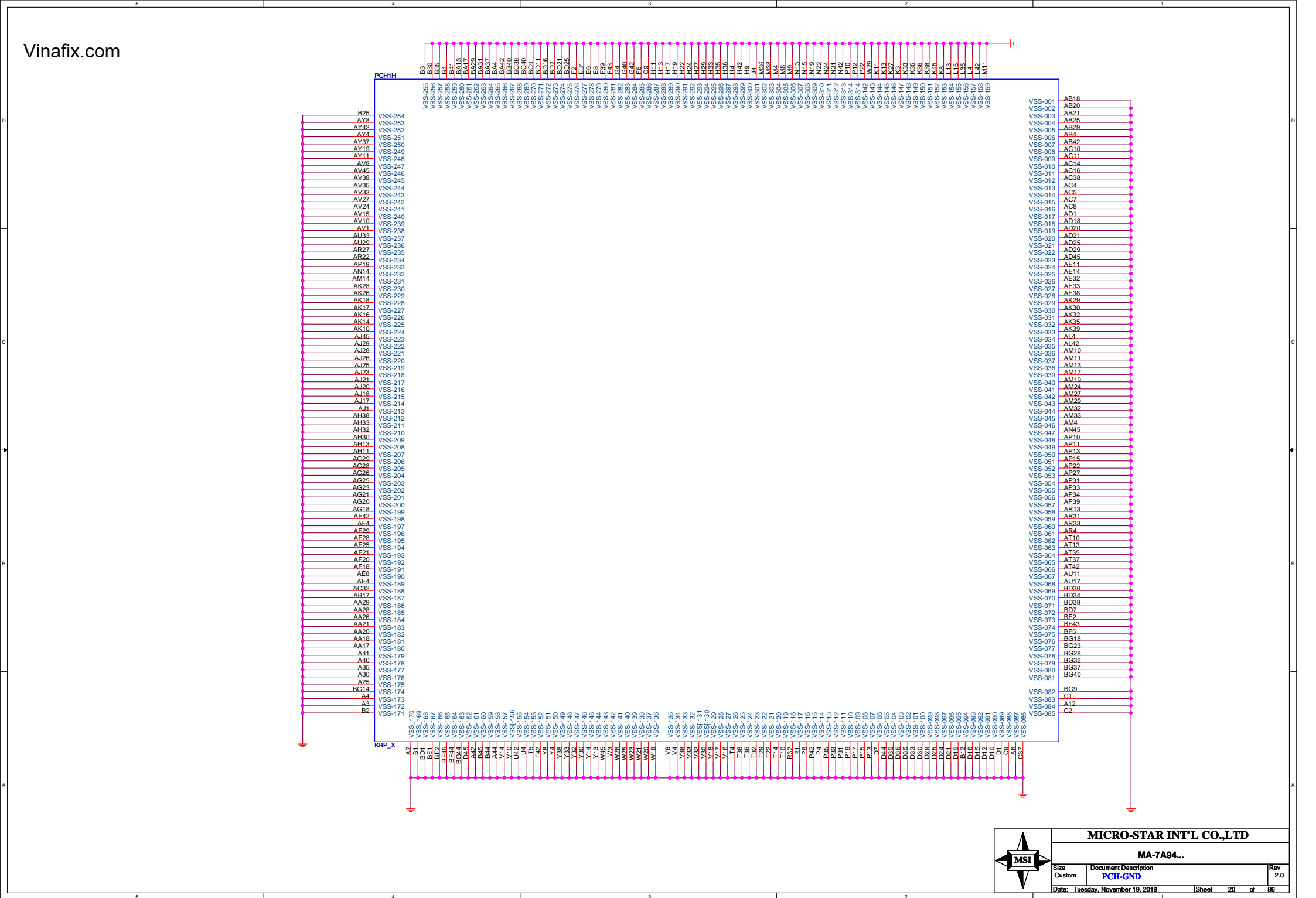
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Used ESPI(GPPA) GPIO Group A will be come 1.8V leve)









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MA-7A94...

Size	Document Description	Rev
Custom	PCB-GND	2.0
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TOP SWAP OVERRIDE STRAP

HIGH: TOP_SWAP ENABLED
LOW : TOP_SWAP DISABLED

PCH HAS INTERNAL WEAK PD

No Reboot OPTION

0 : NO-REBOOT (Default)
1 : REBOOT

PCH HAS INTERNAL WEAK PD

AMT and SBA with confidentiality

0 : DISABLE
1 : ENABLE (Default)

DCI ENABLE

0 : DCI DISABLE
1 : DCI ENABLE (Default)

PCH HAS INTERNAL WEAK PD

CRB

Booot-HALT SEL STRAP

PCH HAS INTERNAL WEAK PU

Boot BIOS

0 : SPI
1 : LPC

LPC eSPI Mode

0 : LPC
1 : eSPI

DISPLAY PORT

0 : DISPLAY NOT DETECTED (Default)
1 : DISPLAY DETECTED

JTAG ODT SEL

HIGH: JTAG ODT ENABLED
LOW : JTAG ODT DISABLED

PCH HAS INTERNAL WEAK PU

ESPI FLASH SHARING MODE

0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

PCH HAS INTERNAL WEAK PD

CONSENT

0 : CONSENT STRAP ENABLE
1 : CONSENT STRAP ENABLE

PCH HAS INTERNAL WEAK PU

DFX TEST MODE

UNSRUFF: NORMAL
STUFF: TEST MODE

PERSONALITY

HIGH: PERSONALITY ENABLED
LOW : PERSONALITY DISABLED

PCH HAS INTERNAL WEAK PU

HDA_SDO

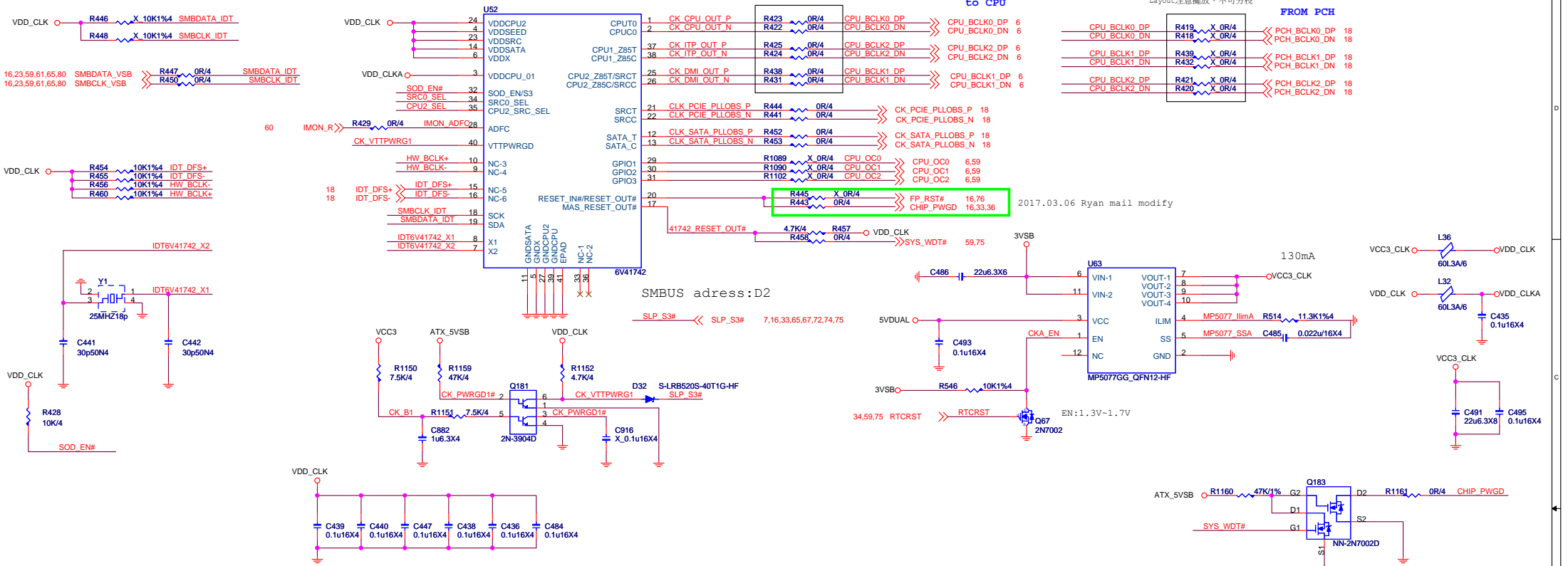
0 : SECURITY MEASURES OVERRIDEN
1 : SECURITY PER FLASH DESCRIPTOR

RING OSCILLATOR BYPASS (DFX)

0 : Ring Oscillator bypass
1 : Normal Mode

XTAL INPUT FREQUENCY [HVM MODE]

BCLK OC



3,18,26,27,61,65,67,78,80 H_PROC_ID1 >> G2 SRC0_SEL

CPU2_SEL D1

3,18,26,27,61,65,67,78,80 H_PROC_ID1 >> G1 H_PROC_ID1

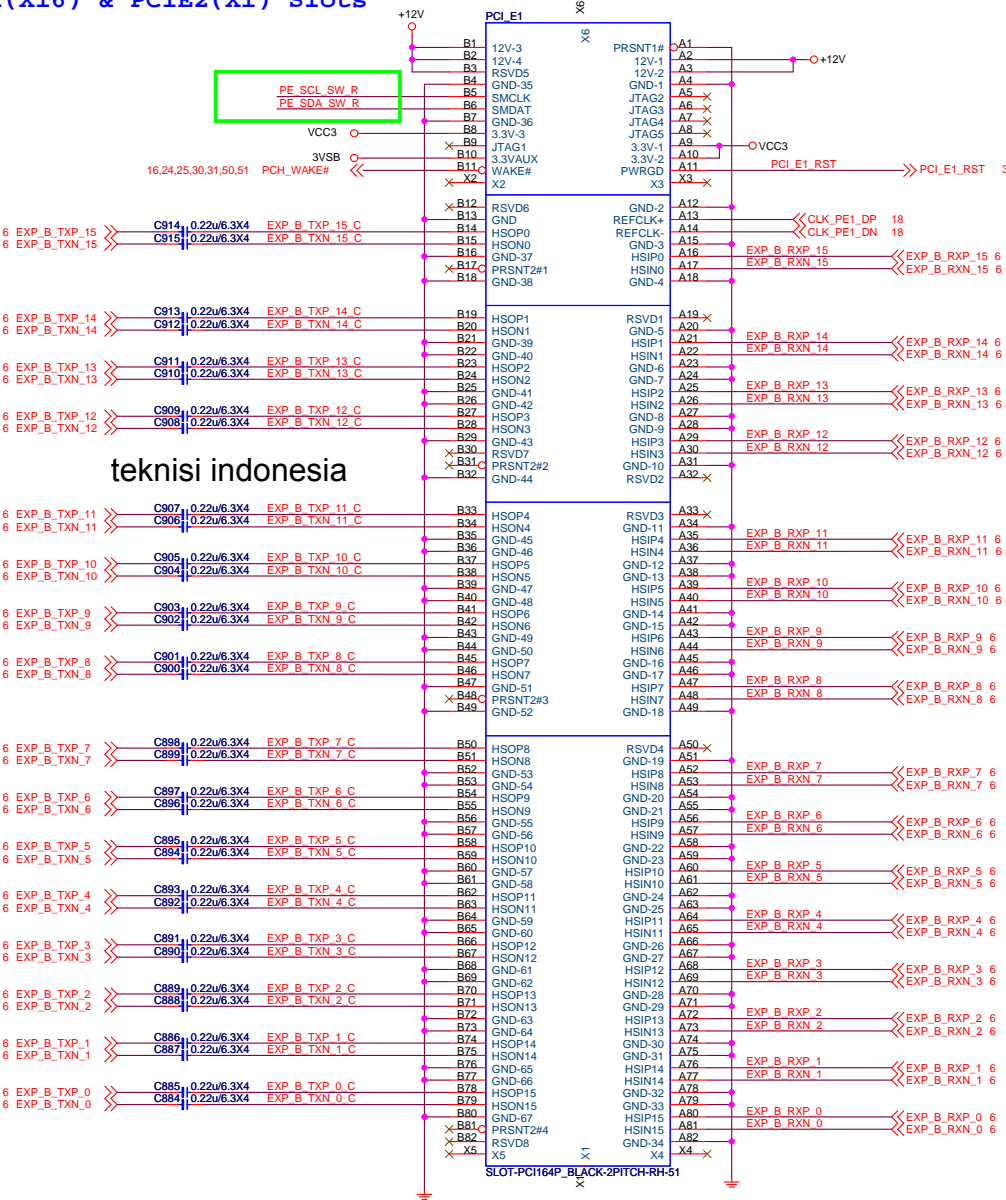
VDD_CLK R413 4.7K/4 SRC0_SEL

VDD_CLK R406 4.7K/4 CPU2_SEL

SRC0_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

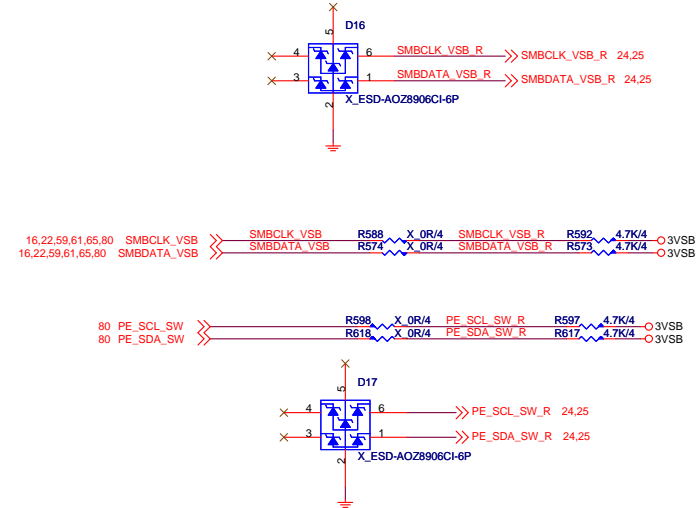
CPU2_SRC_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

PCIE1(X16) & PCIE2(X1) Slots

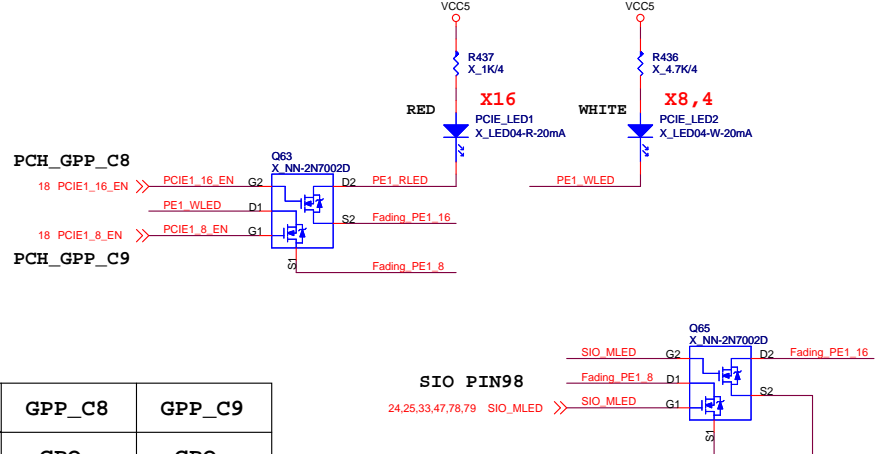


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SMBUS ESD



PCIE SLOT LED

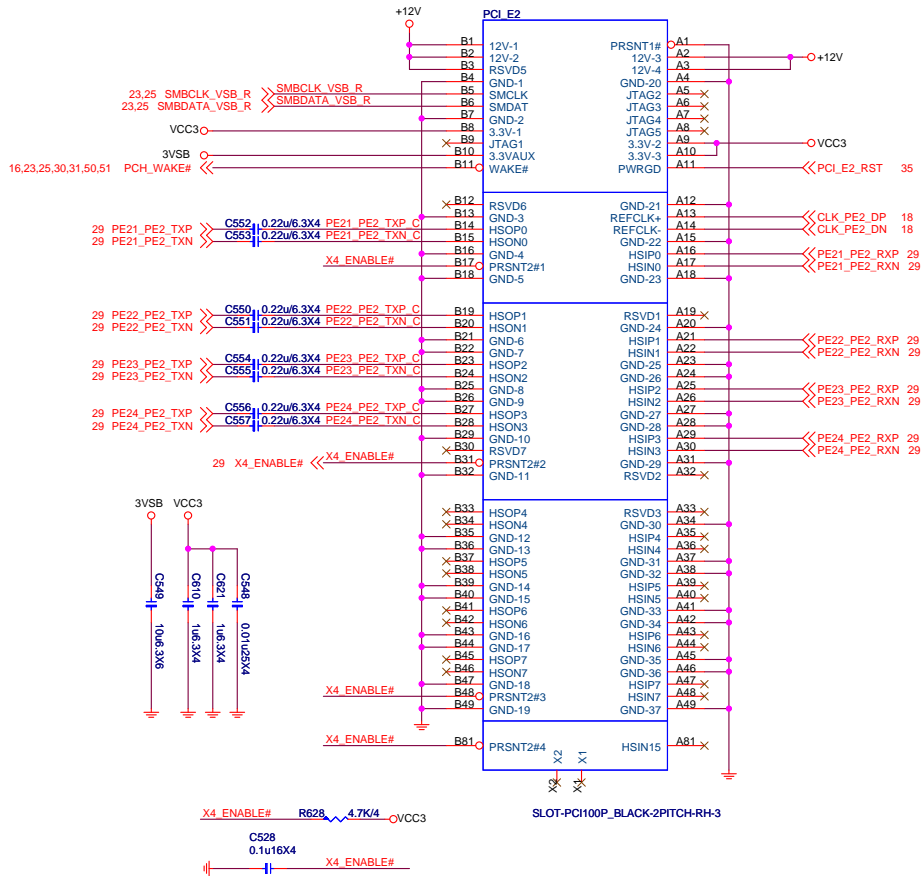


GPIO	GPP_C8	GPP_C9
LED	GPO	GPO
亮	PO HIGH	PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

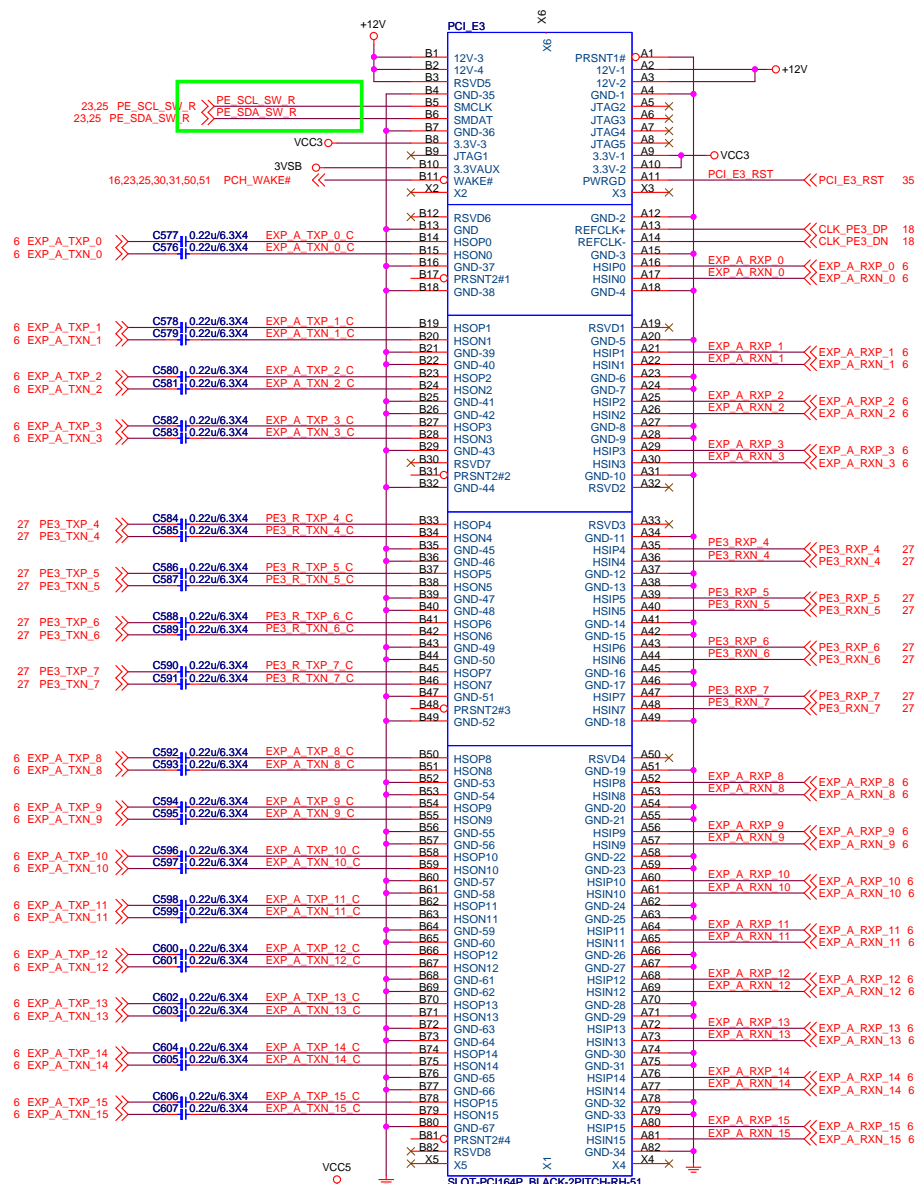
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Size	Document Description	Rev
Custom	PCIE1(X16)	2.0
Date: Tuesday, November 19, 2019A		Sheet 23 of 86

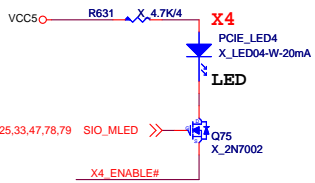


SKL	KBL
PE1 4	PE3 15
PE1 5	PE3 14
PE1 6	PE3 13
PE1 7	PE3 12

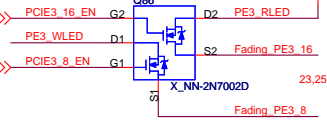


PCIE SLOT LED

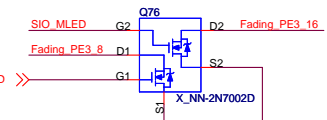
GPIO	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)



PCH_GPP_C8
18 PCIE3_16_EN
PCH_GPP_C9
18 PCIE3_8_EN



SIO PIN98
23,25,33,47,78,79 SIO_MLED



WHITE
X8, 4
PCIE_LED6
X_LED04-W-20mA

RED
X16
PCIE_LED5
X_LED04-R-20mA

PCIE_LED4
X_LED04-W-20mA
LED

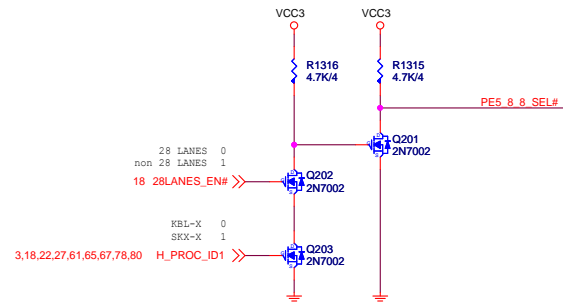
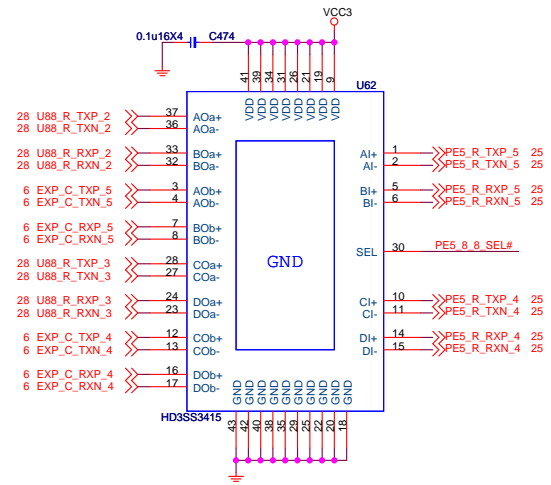
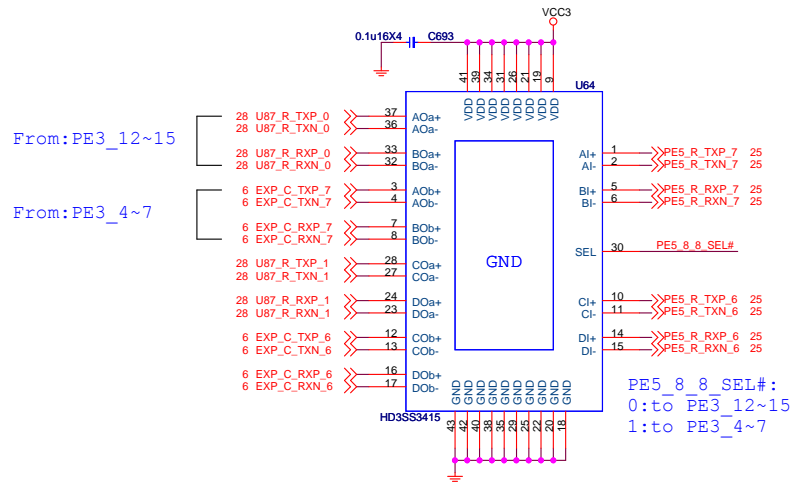
PCIE_LED5
X_LED04-R-20mA
LED

PCIE_LED6
X_LED04-W-20mA
LED



MICRO-STAR INT'L CO.,LTD		
MA-7A94...		
Size	Document Description	Rev
Custom	PCIE2(X4) & PCIE3(X16)	2.0
Date: Tuesday, November 19, 2019	Sheet 24 of 86	

SEL:
0 : 28/16
1 : 44

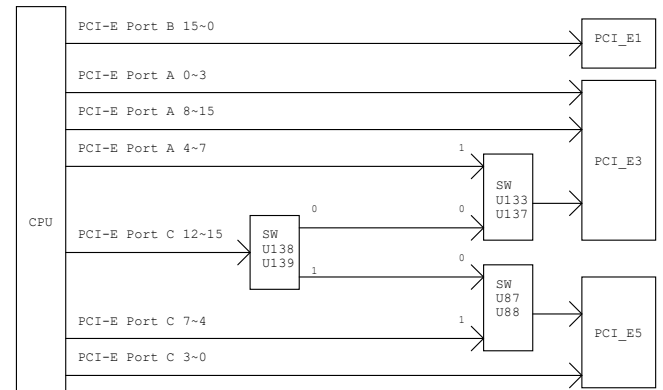


H_PROC_ID1	28LANES_EN#	PE5_8_8_SEL#
1	1	1
1	0	0
0	1	0

44Lanes

28Lanes

16Lanes

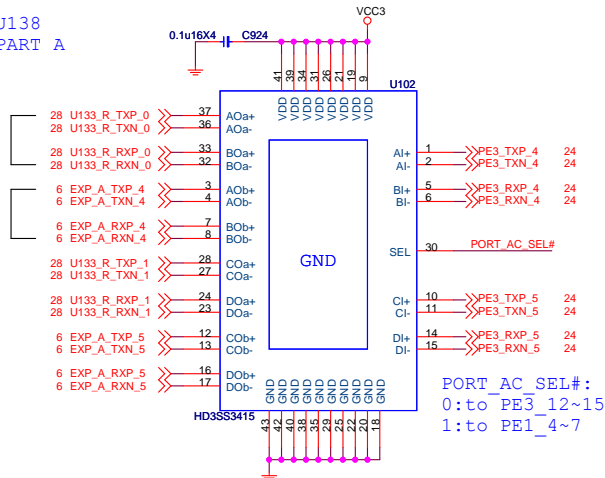


	SKL-X 44L	SKL-X 28L	KBL-X			
PE1	X16:P2[15:0]	X16:P2[15:0]	X8:P2[15:8]	X8:P2[15:8]		
PE3	X16:P1[0:15]	X8:P1[0:7]	X4:P1[0:3]	X8:P2[0:3]+P3[15:12]		
PE5	X8:P3[7:0]	X4:P3[15:12]	X4:P3[15:12]	X0:		
PE4	PCH_PE3	PCH_PE3	PCH_PE3	PCH_PE3		
M2_1	PCH_PE9~12	PCH_PE9~12	PCH_PE9~12	PCH_PE9~12		
M2_2	PCH_PE17~20	PCH_PE17~20	PCH_PE17~20	PCH_PE17~20		
PE2	PCH_PE21~24	PCH_PE21~24	PCH	PCH	PCH	PCH
U.2	PCH_PE21~24	PCH_PE21~24	PCH	PCH	PCH	PCH

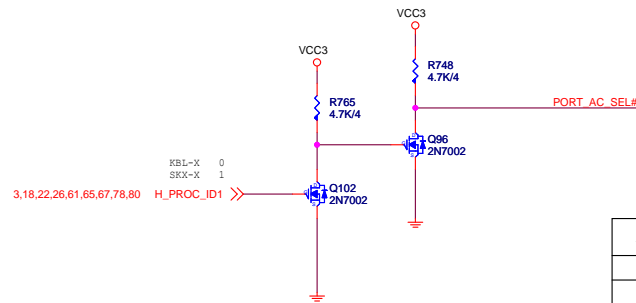
SEL:
0:from U138
1:from PART A

From:PE3_12~15

From:PE1_4~7

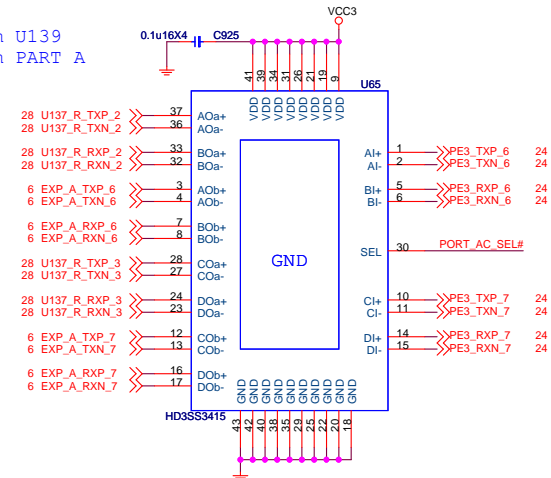


PORT_AC_SEL#:
0:to PE3_12~15
1:to PE1_4~7



SEL:
0:16 x8
1:44/28/16 x4

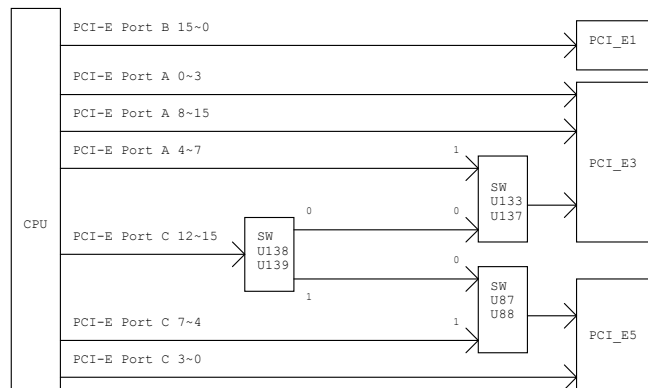
SEL:
0:from U139
1:from PART A



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H_PROC_ID1	PORT_AC_SEL#
1	1
0	0

SKL-X
KBL-X



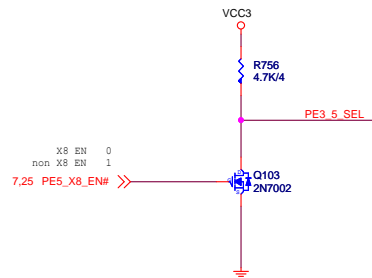
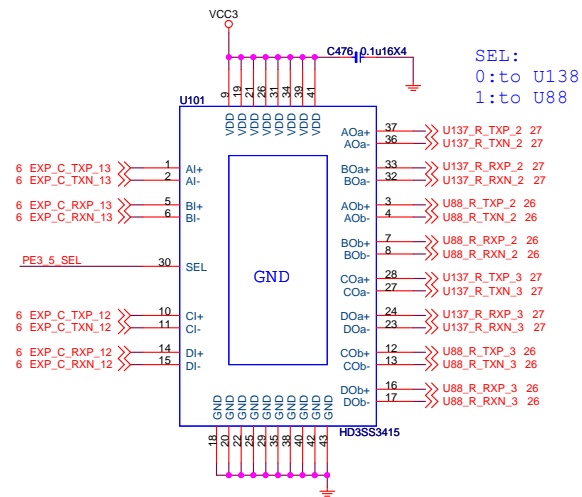
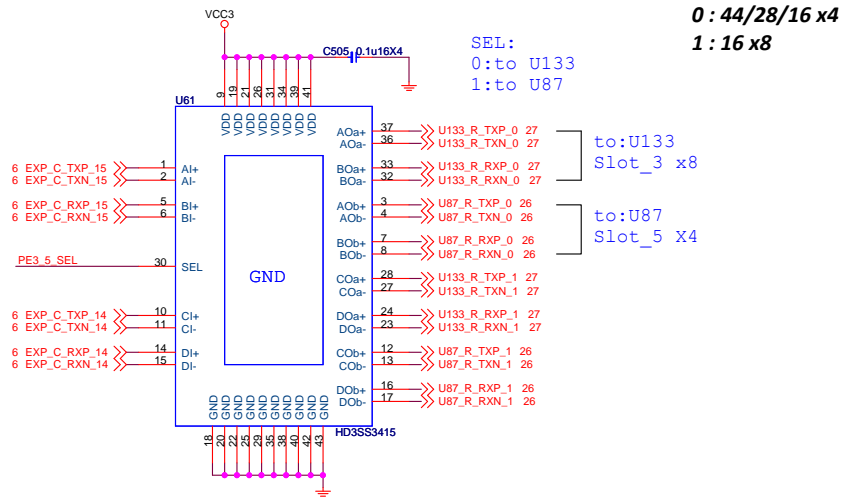
	SKL-X 44L	SKL-X 28L	KBL-X			
PE1	X16:P2[15:0]	X16:P2[15:0]	X8:P2[15:8]	X8:P2[15:8]		
PE3	X16:P1[0:15]	X8:P1[0:7]	X4:P1[0:3]	X8:P2[0:3]+P3[15:12]		
PE5	X8:P3[7:0]	X4:P3[15:12]	X4:P3[15:12]	X0:		
PE4	PCH_PE3	PCH_PE3	PCH_PE3	PCH_PE3		
M2_1	PCH_PE9~12	PCH_PE9~12	PCH_PE9~12	PCH_PE9~12		
M2_2	PCH_PE17~20	PCH_PE17~20	PCH_PE17~20	PCH_PE17~20		
PE2	PCH_PE21~24	---	PCH_PE21~24	---	PCH	---
U.2	---	PCH_PE21~24	---	PCH_PE21~24	---	PCH



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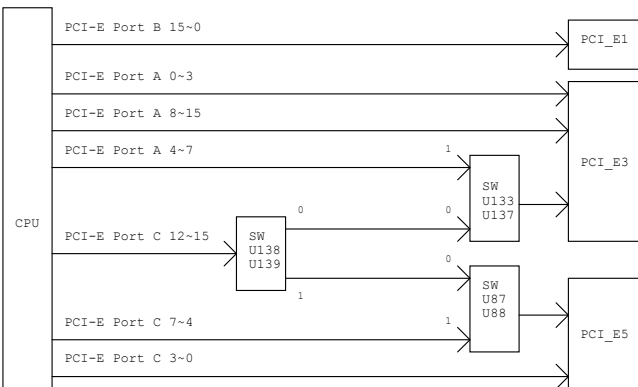
Size Custom	Document Description PCI-E-SWITCH	Rev 2.0
Date: Tuesday, November 19, 2019		
Sheet 27 of 86		



PE5_X8_EN#	PE3_5_SEL
1	0
0	1

PE5 x4 in

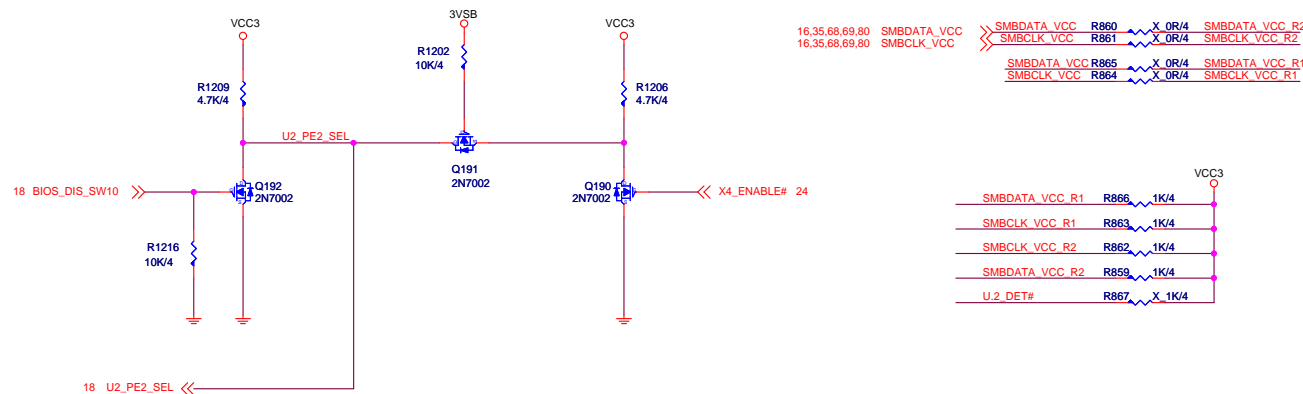
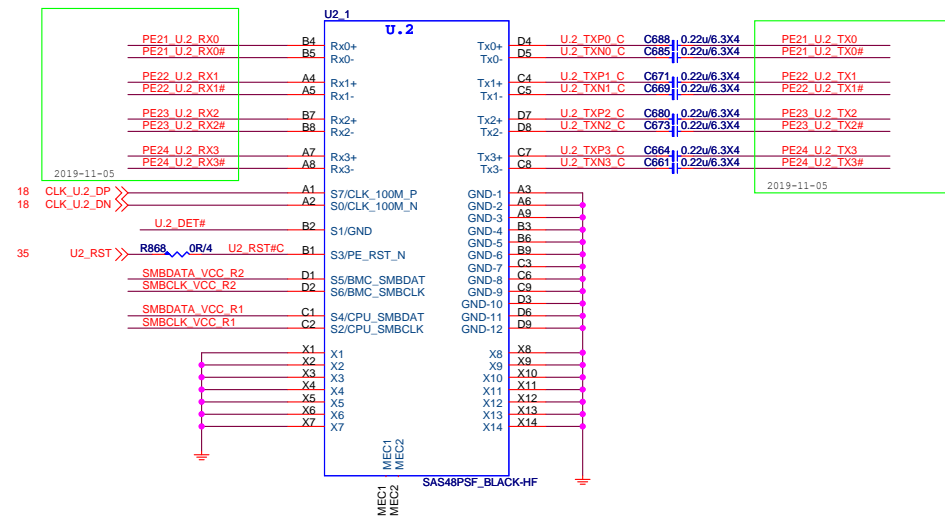
	SKL-X 44L	SKL-X 28L	KBL-X	
PE1	X16:P2[15:0]	X16:P2[15:0]	X8:P2[15:8]	X8:P2[15:8]
PE3	X16:P1[0:15]	X8:P1[0:7]	X4:P1[0:3]	X8:P2[0:3]+P3[15:12]
PE5	X8:P3[7:0]	X4:P3[15:12]	X4:P3[15:12]	X0:
PE4	PCH_PE3	PCH_PE3	PCH_PE3	PCH_PE3
M2_1	PCH_PE9~12	PCH_PE9~12	PCH_PE9~12	PCH_PE9~12
M2_2	PCH_PE17~20	PCH_PE17~20	PCH_PE17~20	PCH_PE17~20
PE2	PCH_PE21~24	PCH_PE21~24	PCH	PCH
U.2	PCH_PE21~24	PCH_PE21~24	PCH	PCH



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MA-7A94...

Size	Document Description	Rev
Custom	SKX/KBX SWITCH	2.0
Date: Tuesday, November 19, 2019	Sheet 28 of 86	

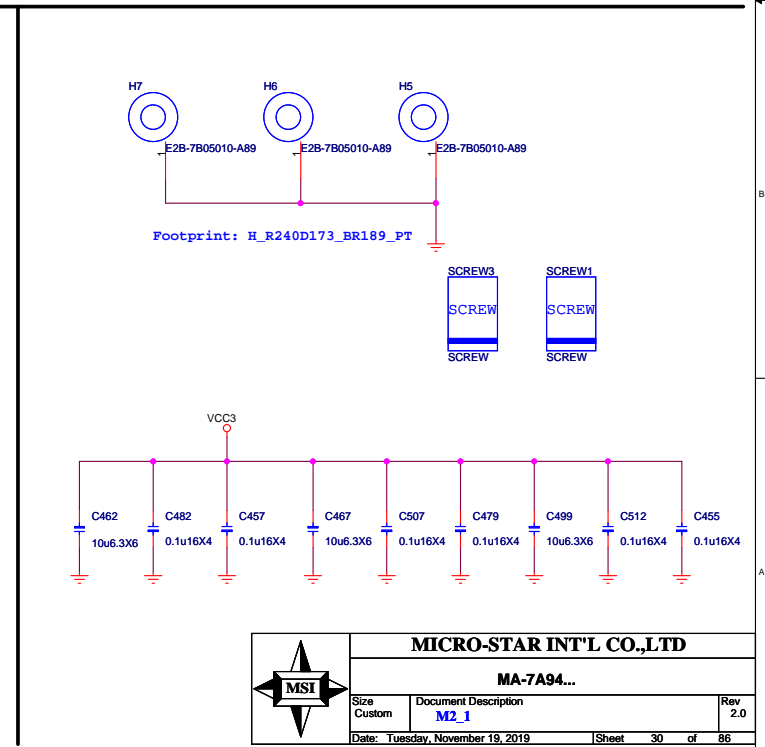
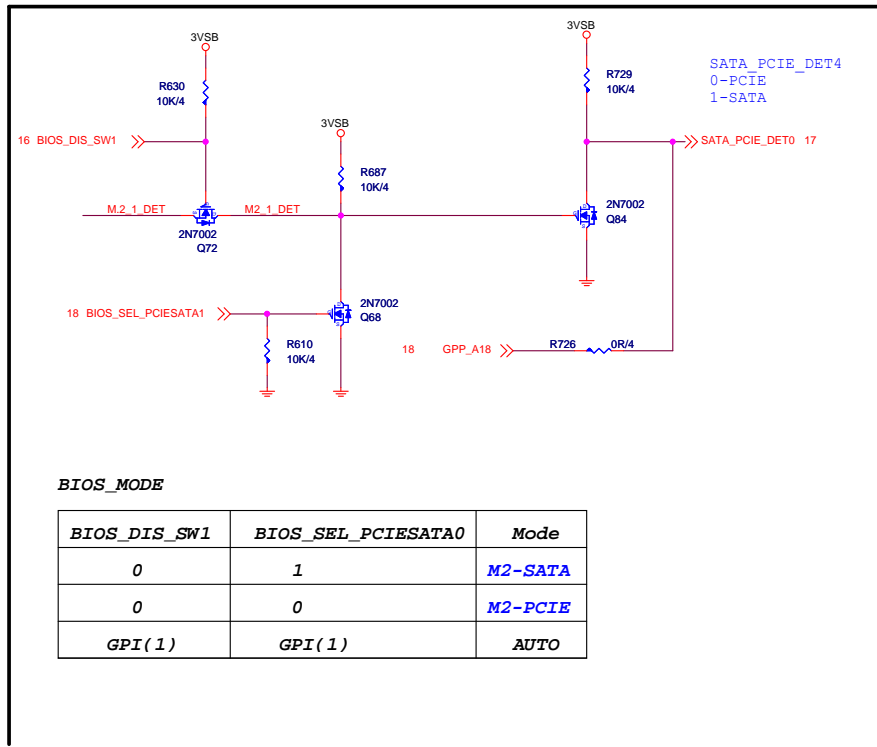
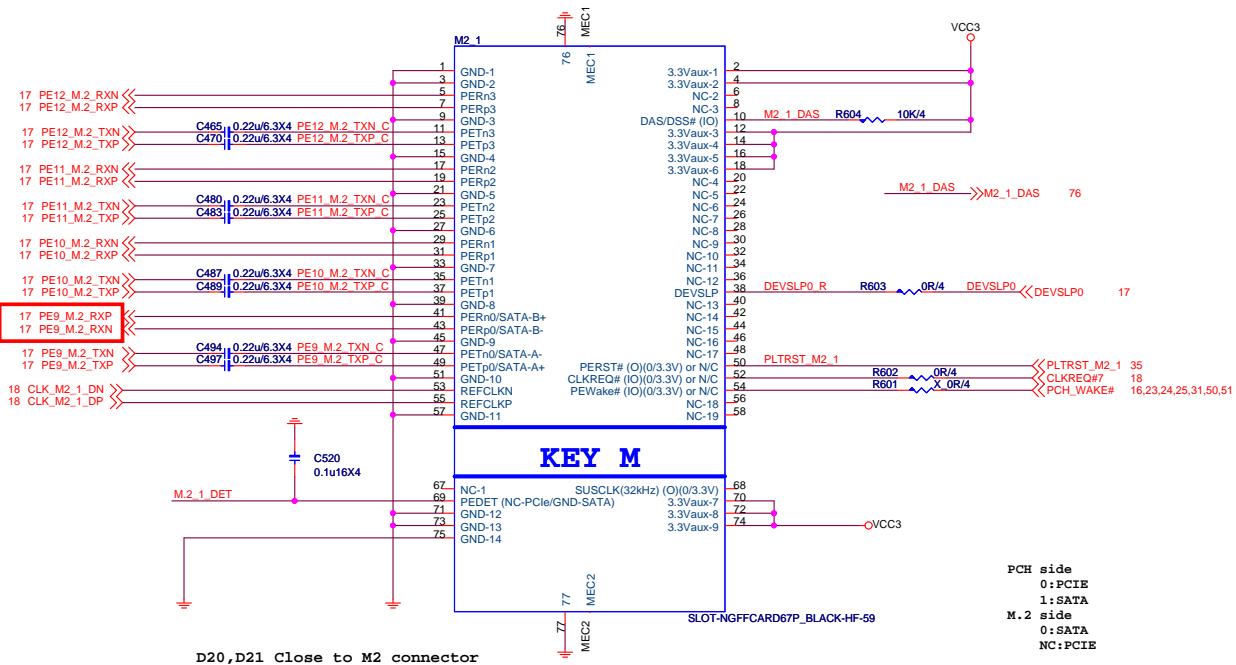


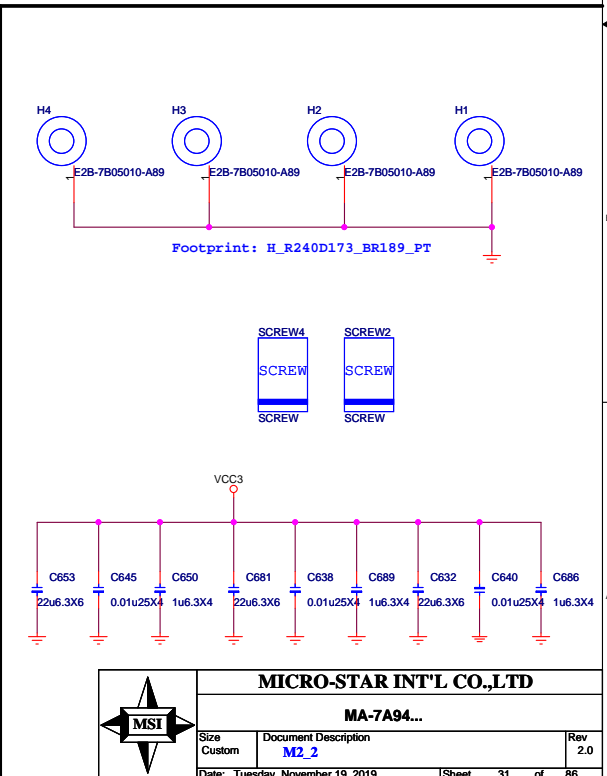
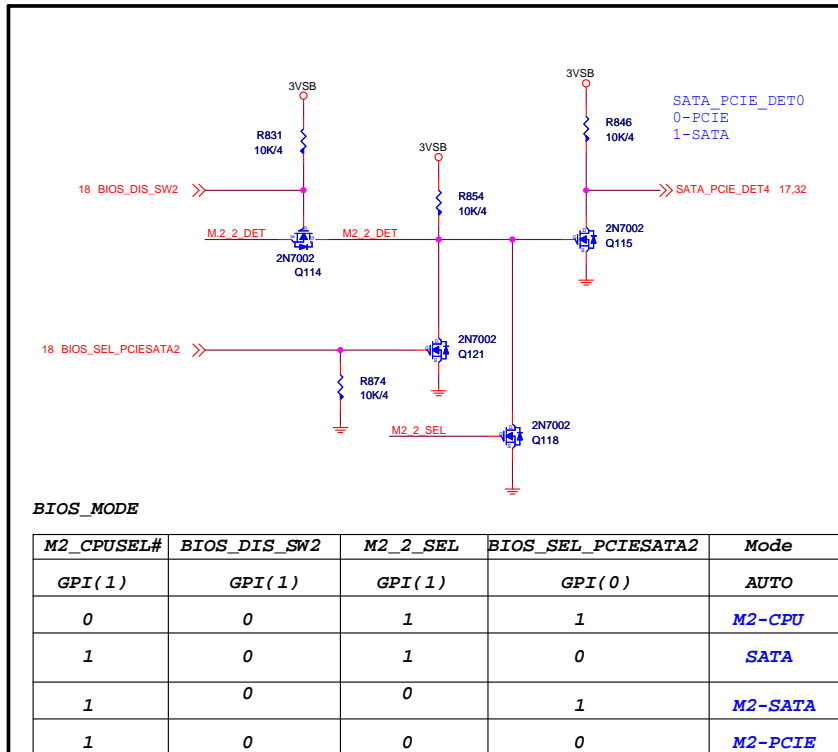
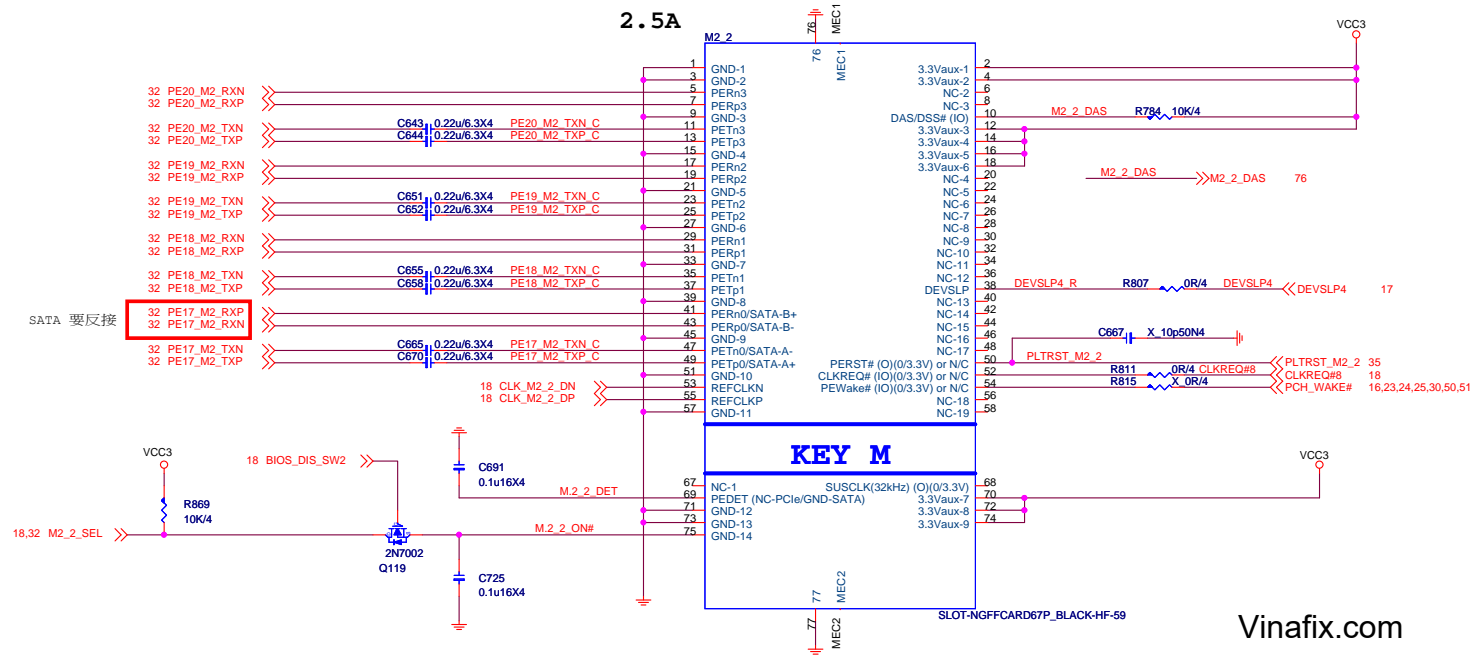
X4_ENABLE#	U2_PE2_SEL
1	0
0	1

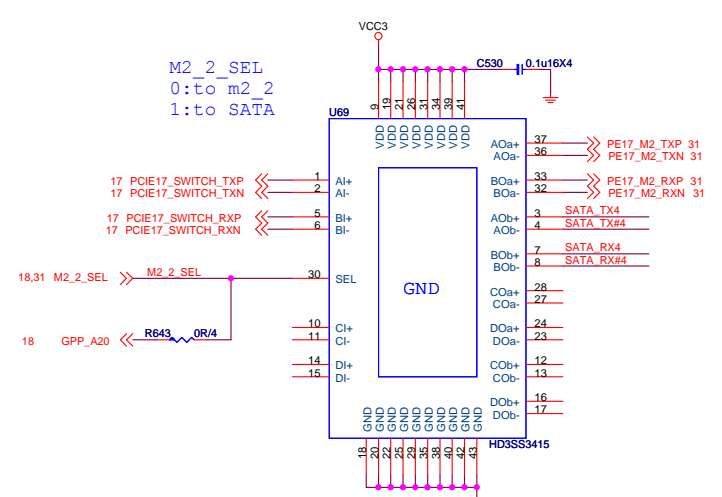
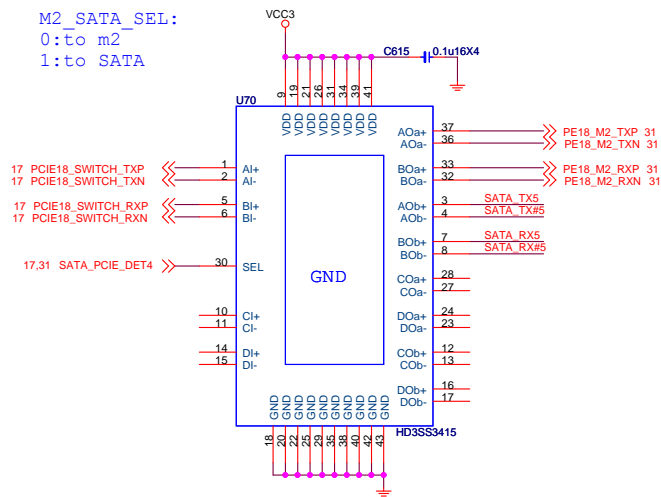
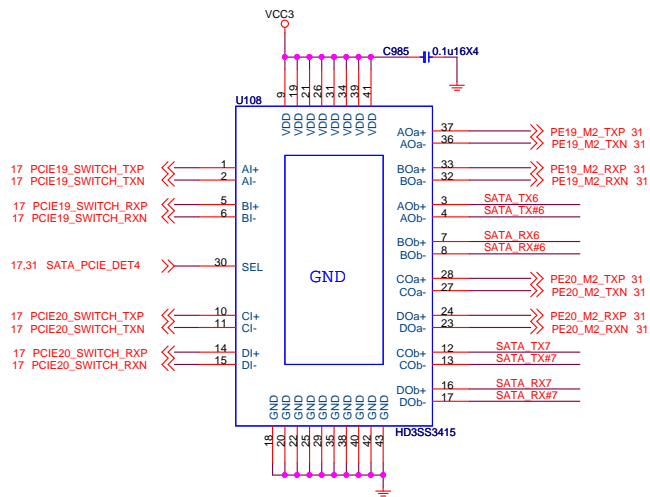
PE2 x4 in



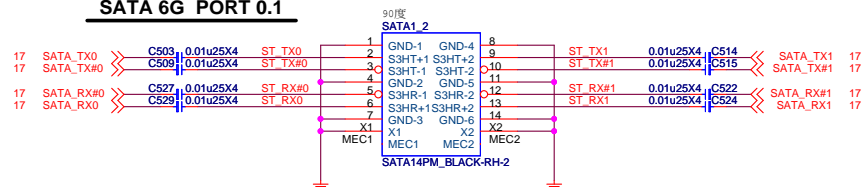
SATA 要反接



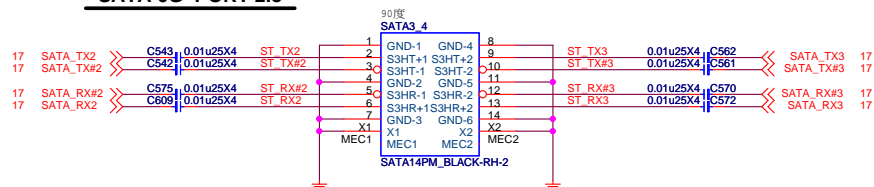




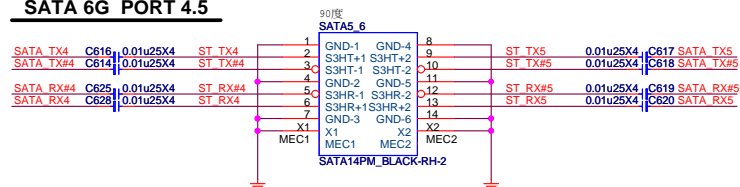
SATA 6G PORT 0.1



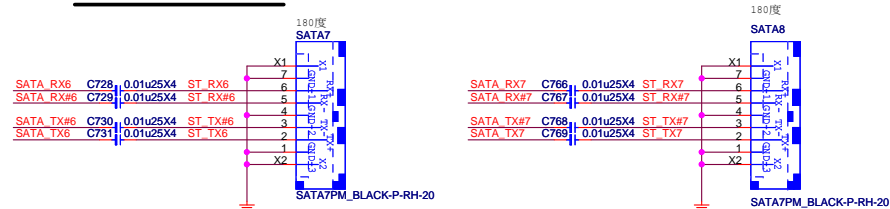
SATA 6G PORT 2.3



SATA 6G PORT 4.5



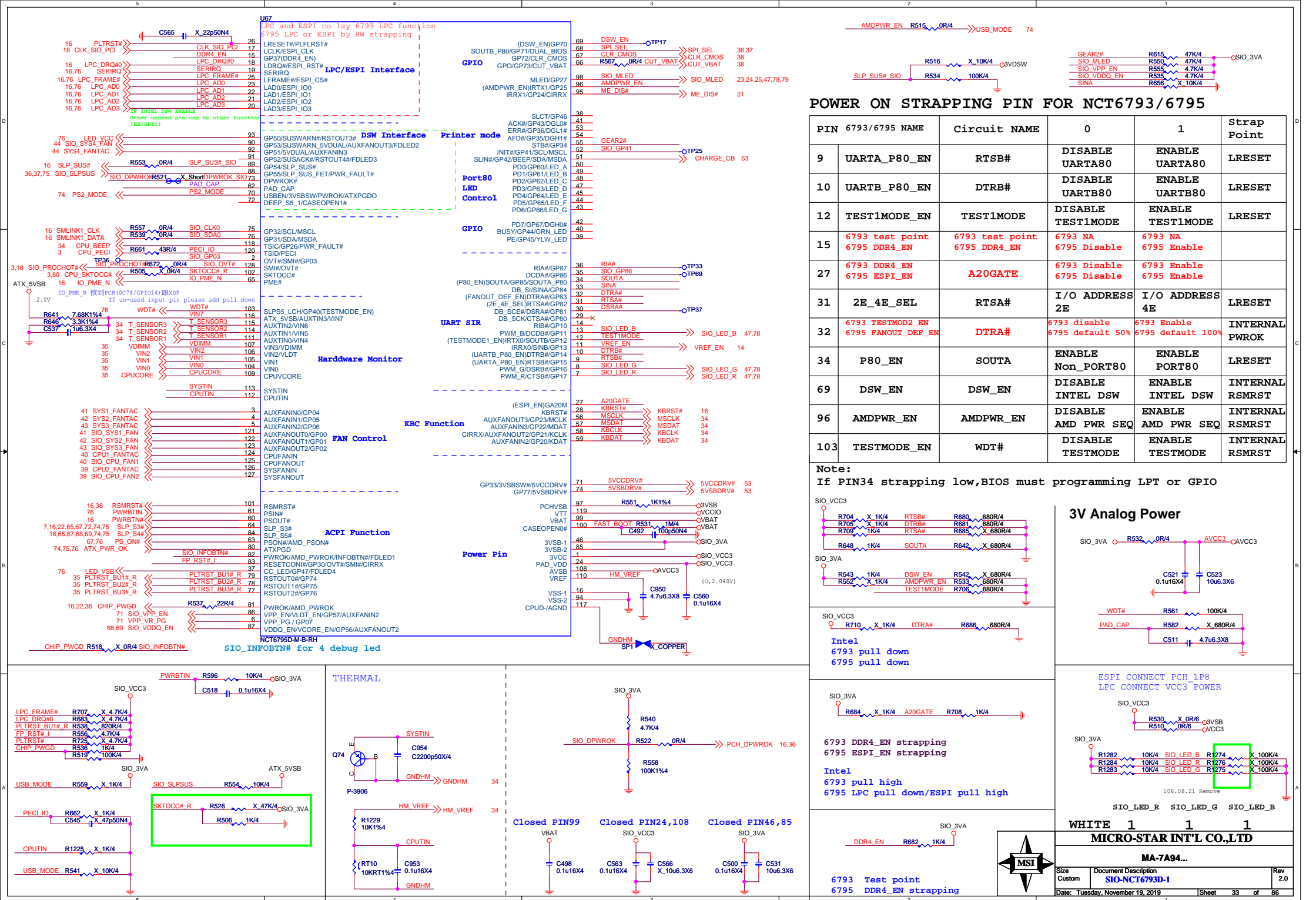
SATA 6G PORT 6.7



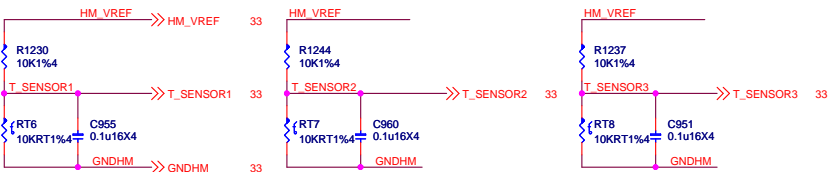
MICRO-STAR INT'L CO.,LTD

MA-7A94...

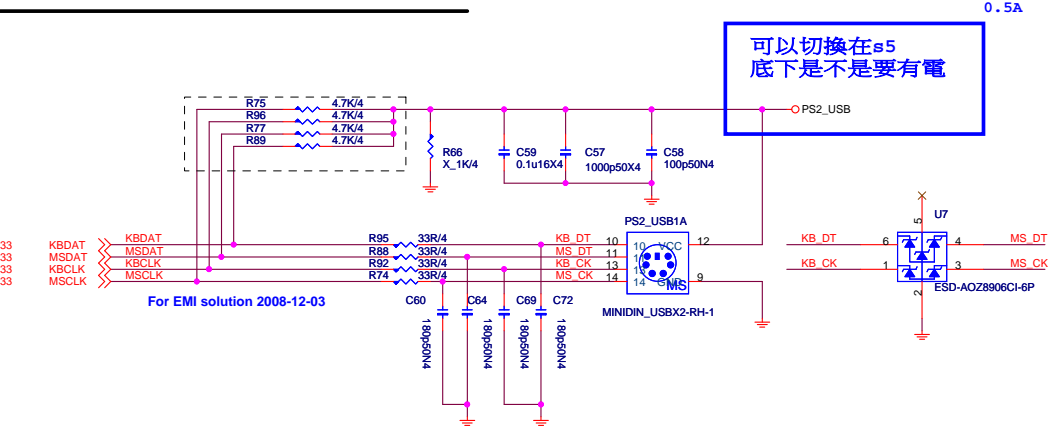
Size	Document Description	Rev
Custom	SATA CONN	2.0
Date: Tuesday, November 19, 2019	Sheet 32 of 86	



THERMAL

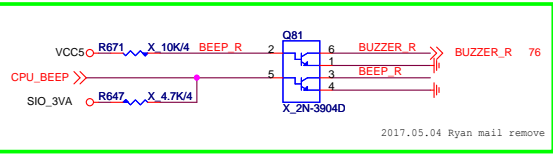


PS2 KEYBOARD & MOUSE CONNECTOR



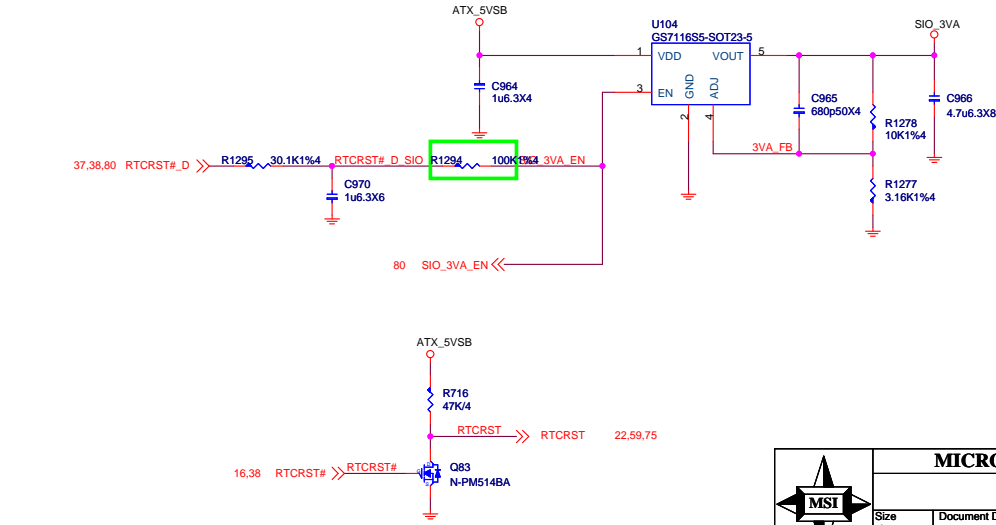
DEBUG LED

COM Port for BIOS Debug



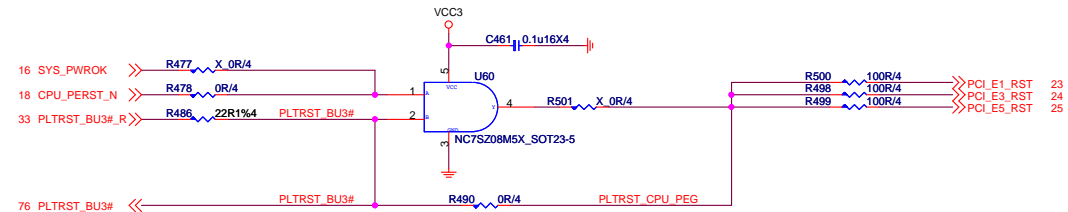
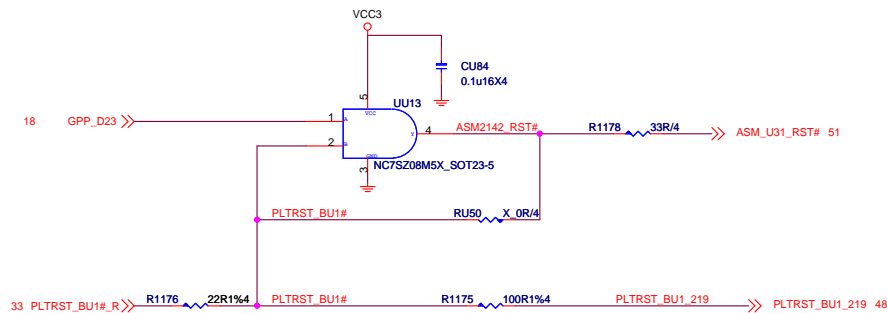
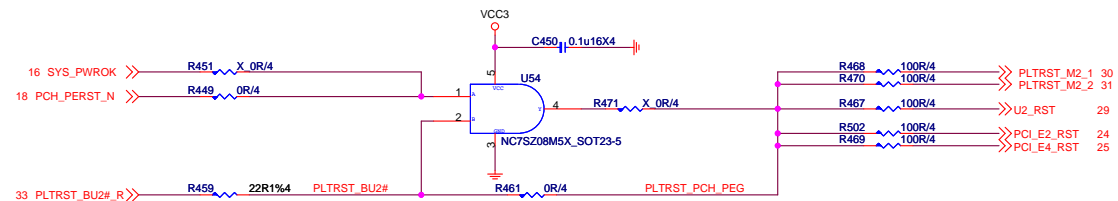
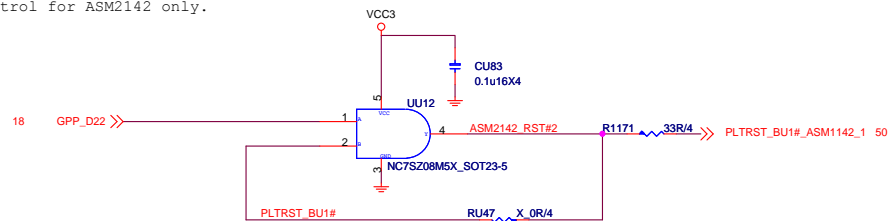
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SLP_SUS Co-lay circuit



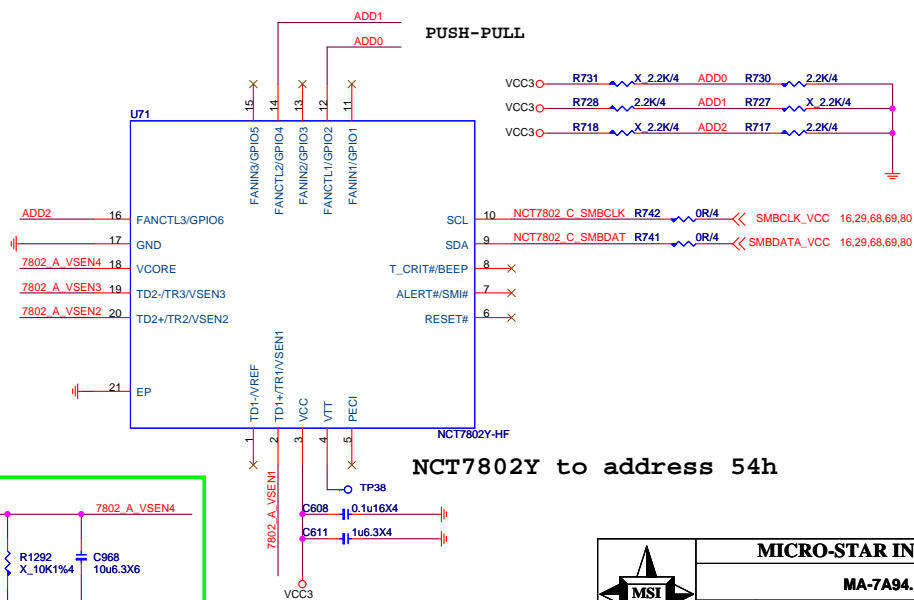
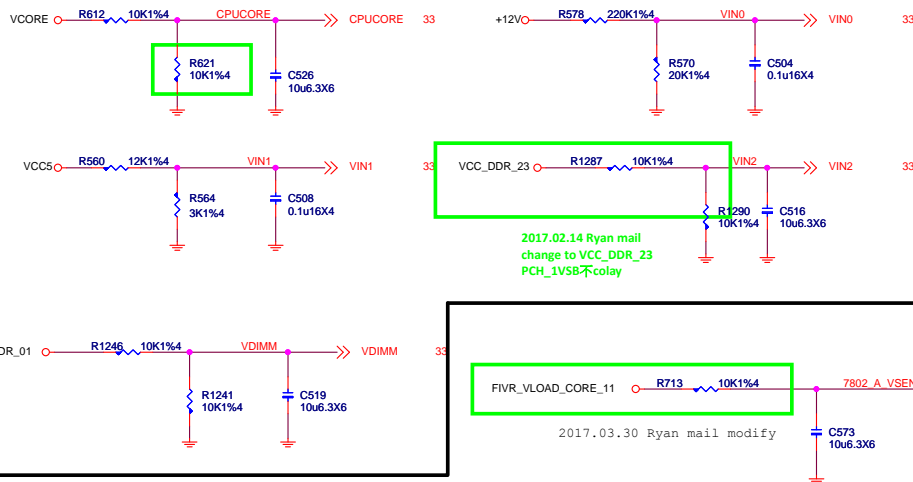
MICRO-STAR INT'L CO.,LTD		
MA-7A94...		
Size Custom	Document Description SIO-NCT6793D-2	Rev 2.0
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Reset control for ASM2142 only.



HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



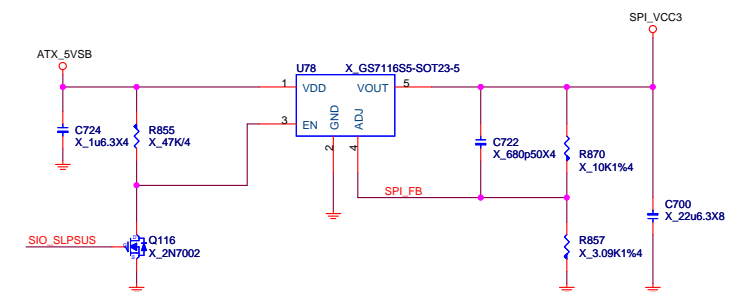
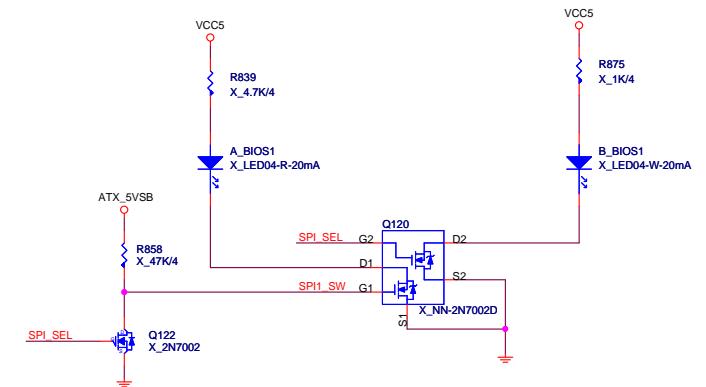
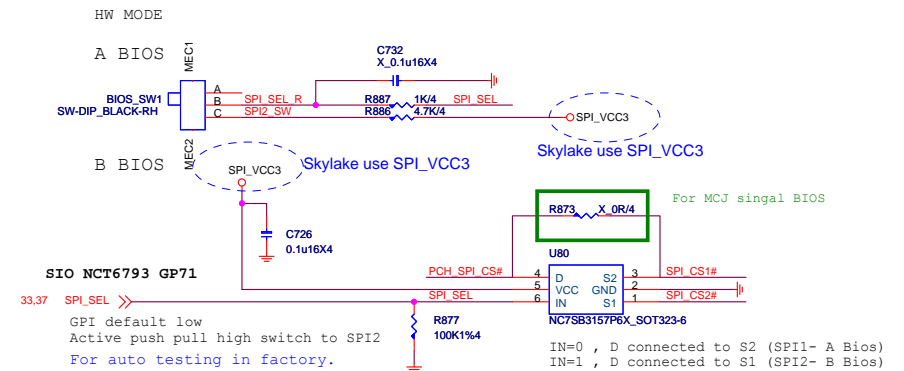
NCT7802Y to address 54h



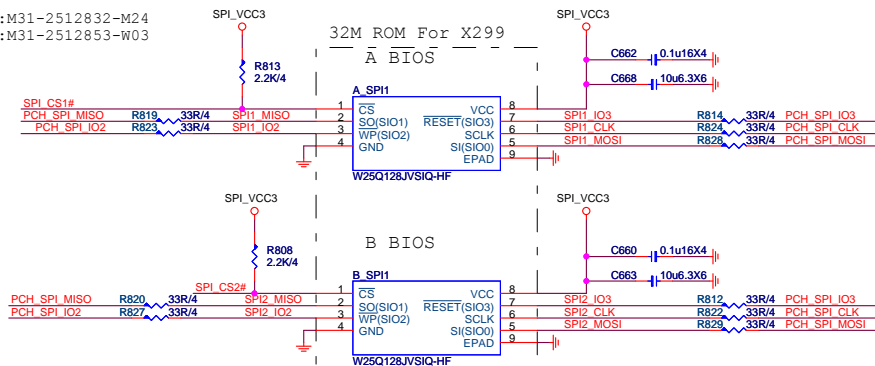
MICRO-STAR INT'L CO.,LTD

MA-7A94...

Size	Document Description	Rev
Custom	SIO-NCT6793D-3	2.0
Date:	Tuesday, November 19, 2019	Sheet 35 of 86



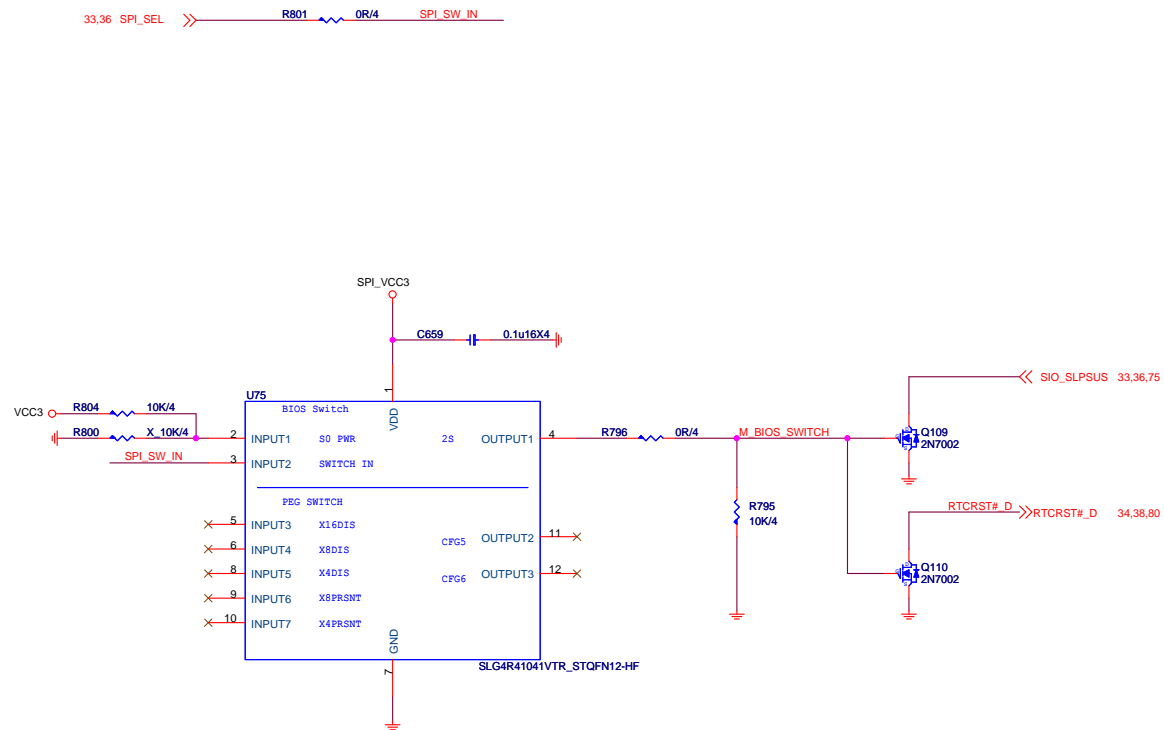
```
MXIC:M31-2512832-M24
WinB:M31-2512853-W03
```



*SPI_CLK & SPI_MOSI must be length matched to within 500mils. < 6 inch
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.



Skylake/Kabylake Path Circuit For Dual Bios



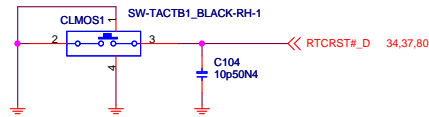
MICRO-STAR INT'L CO.,LTD

MA-7A94...

Size Custom	Document Description Dual bios control-Silego	Rev 2.0
Date: Tuesday, November 19, 2019	Sheet 37 of 86	

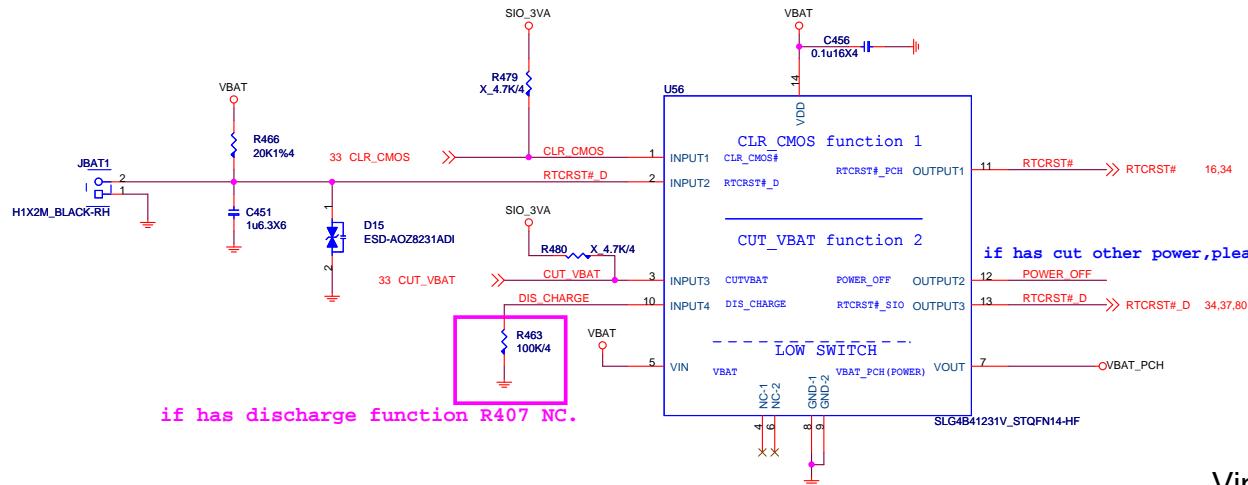
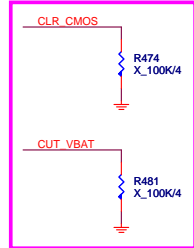
RTCRST# R462 X_0R/4 RTCRST#_D

Clear CMOS button

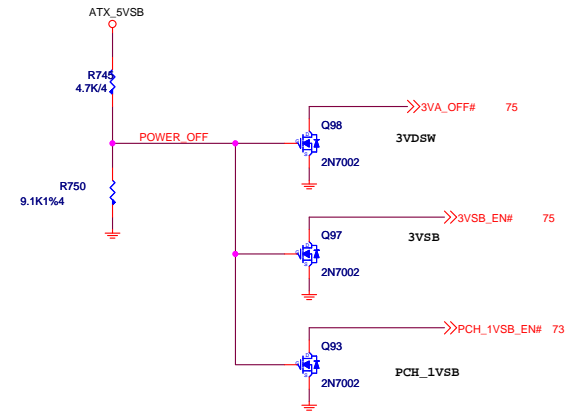


CUT VBAT

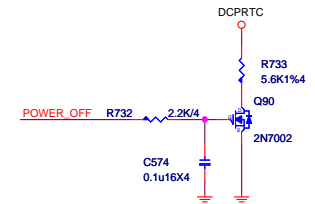
20160629



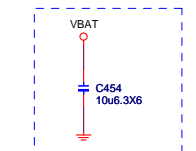
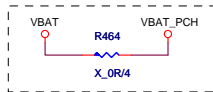
Vinafix.com



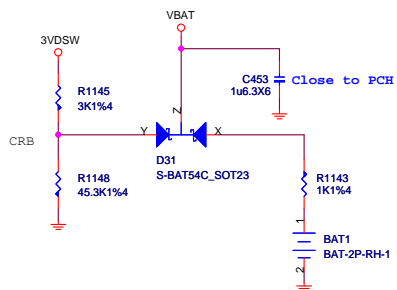
Add DCRTC discharge circuit



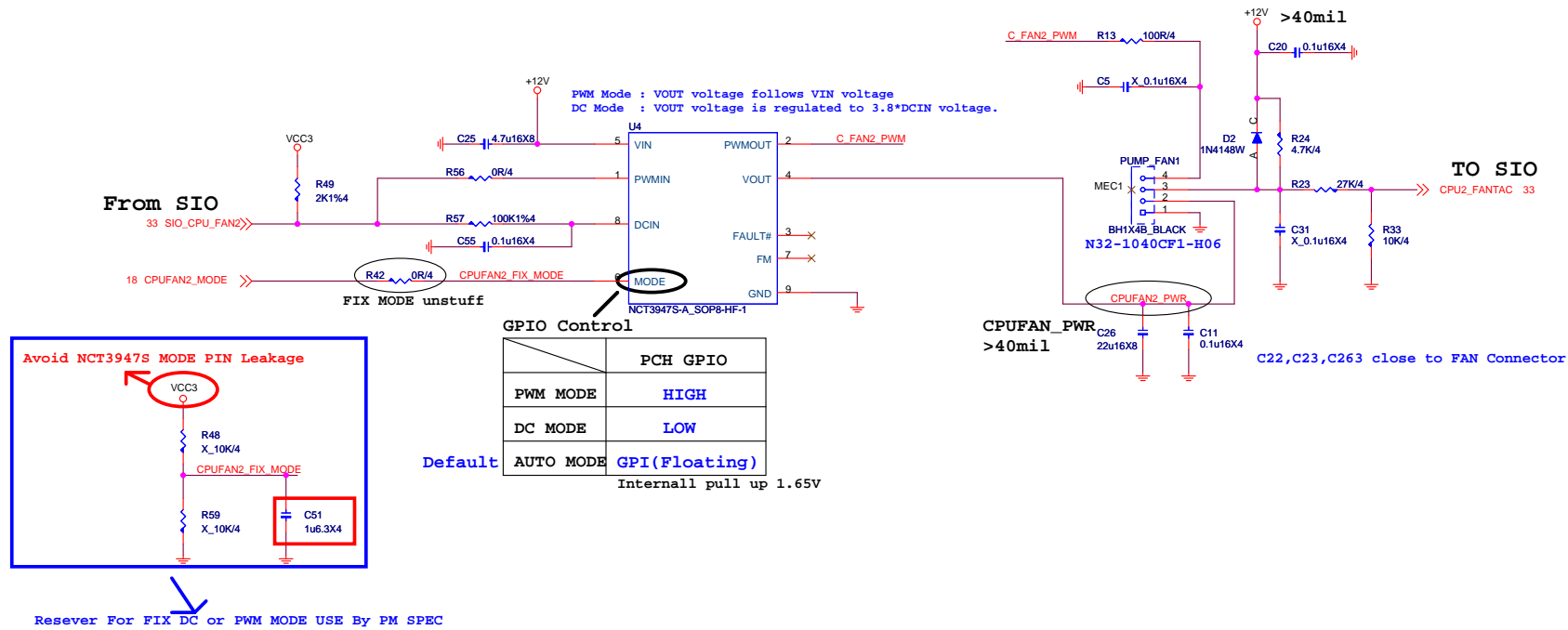
VBAT



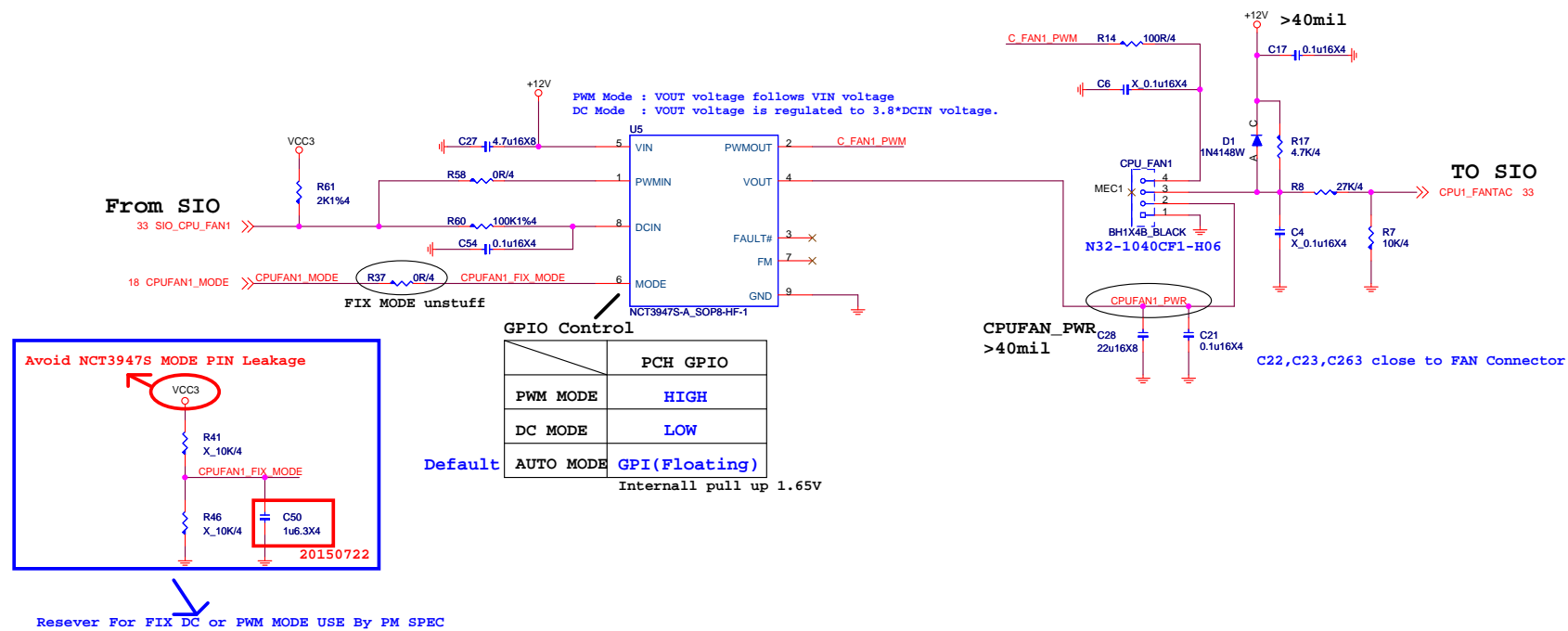
have timing issue keep 0805 size don't removed



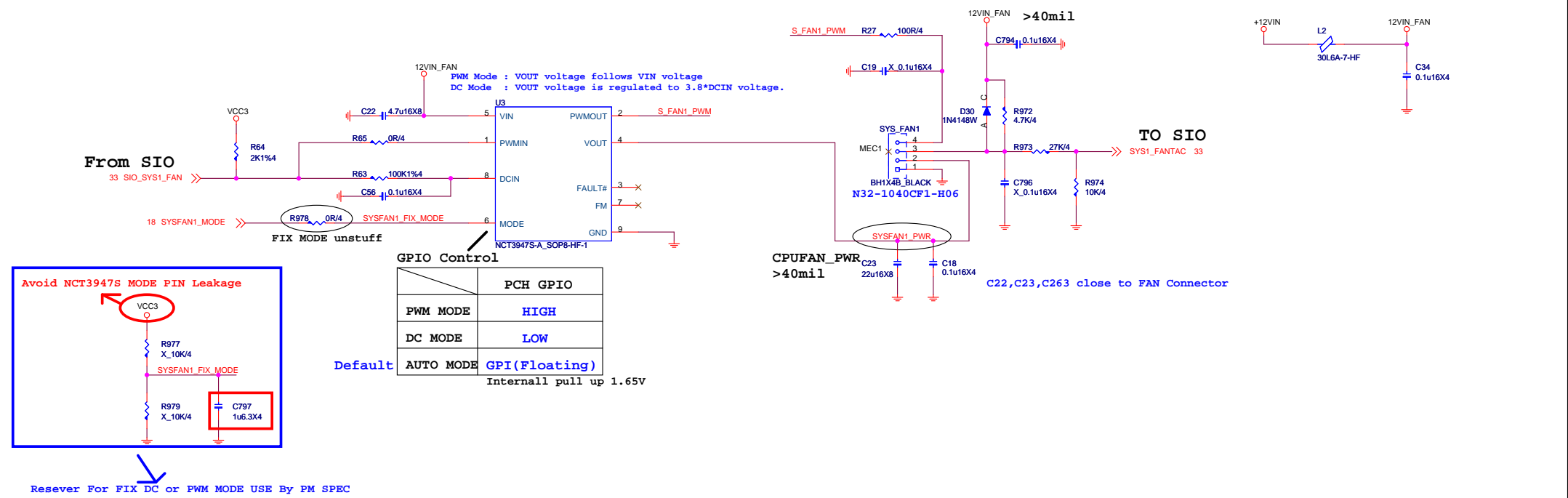
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

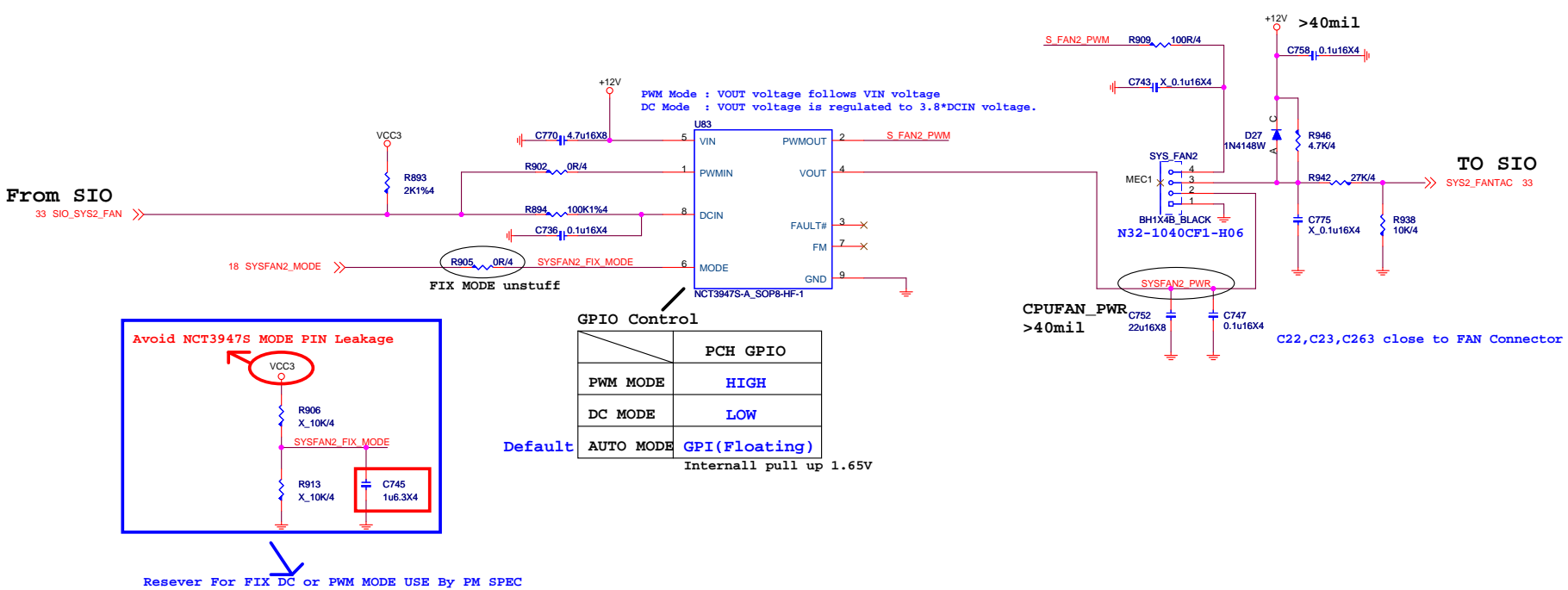


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

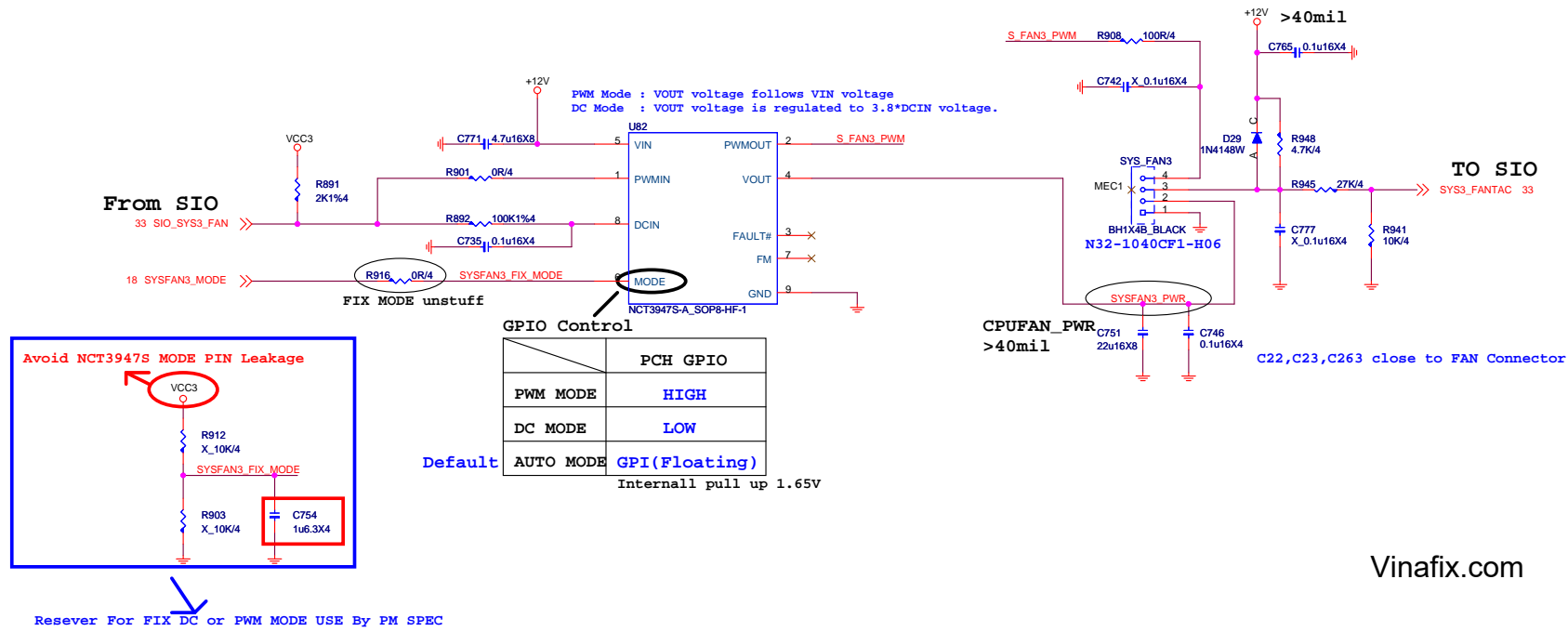


Vinafix.com

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

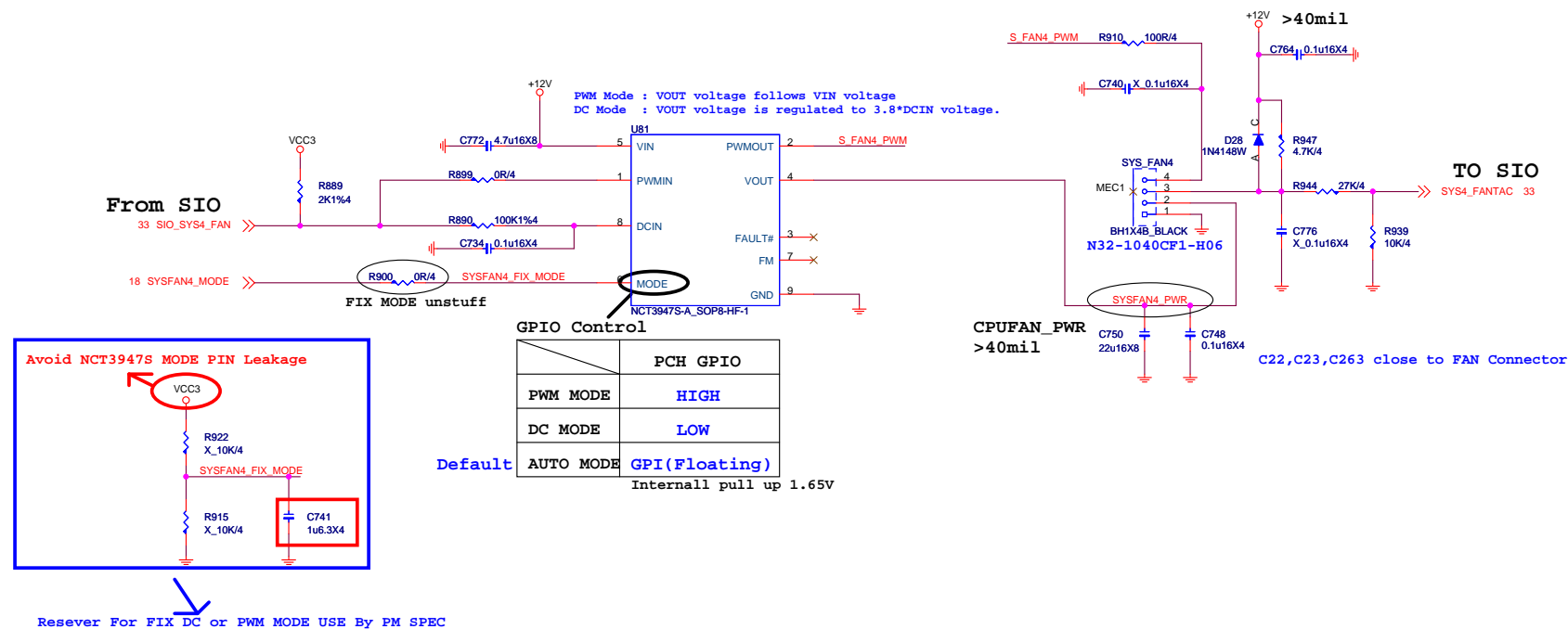


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

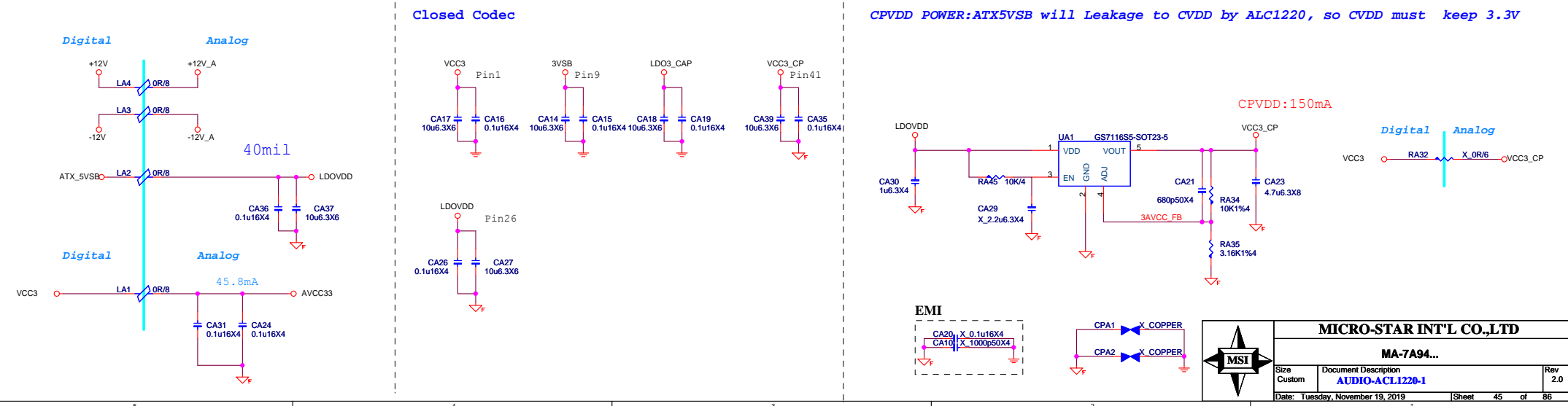
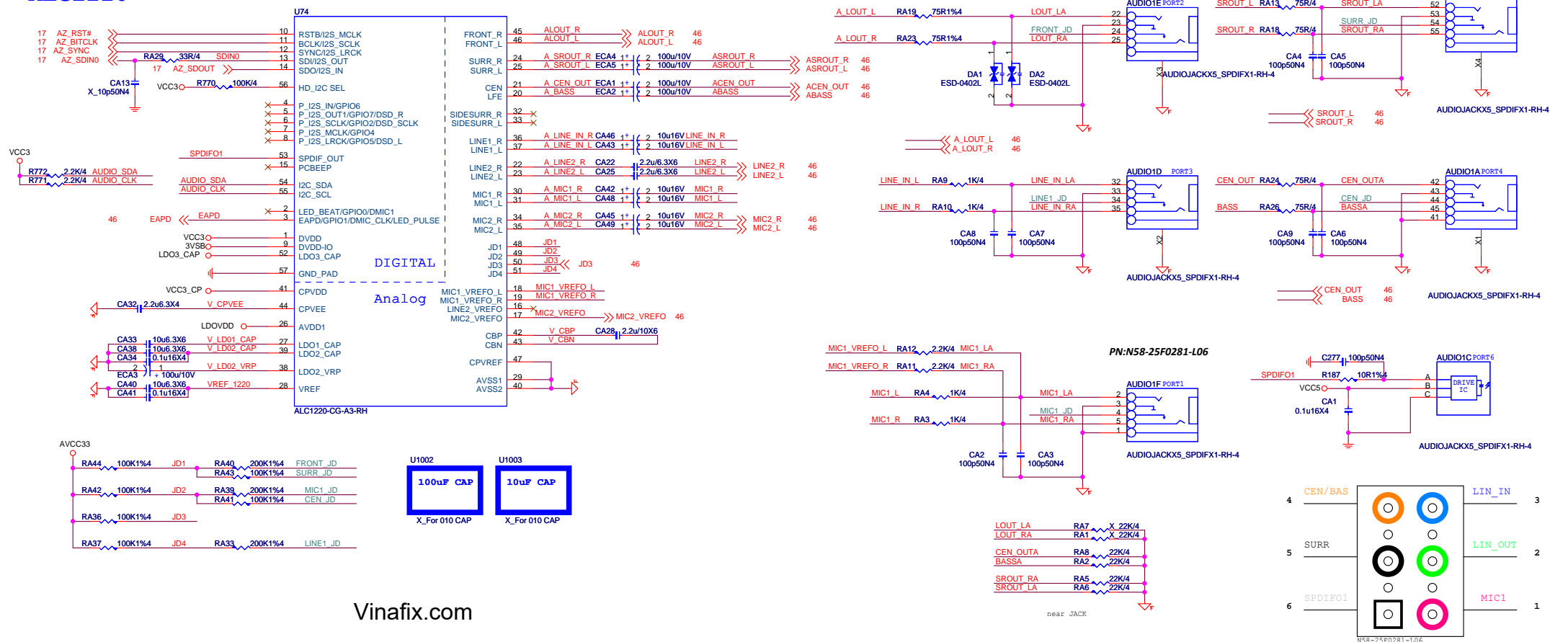


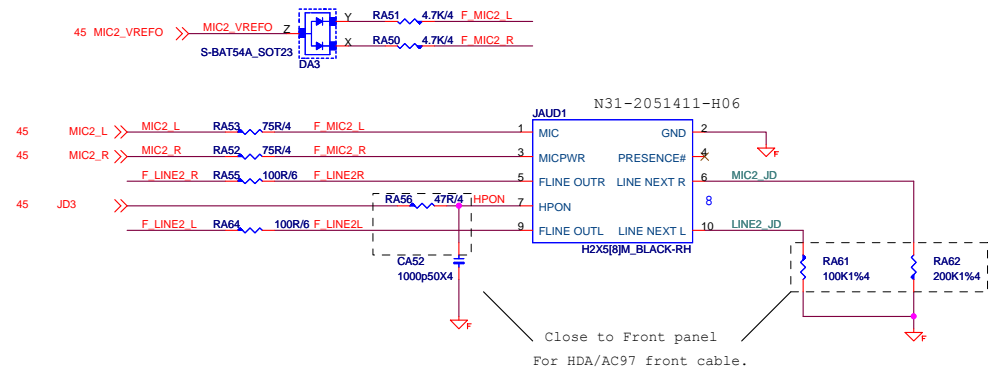
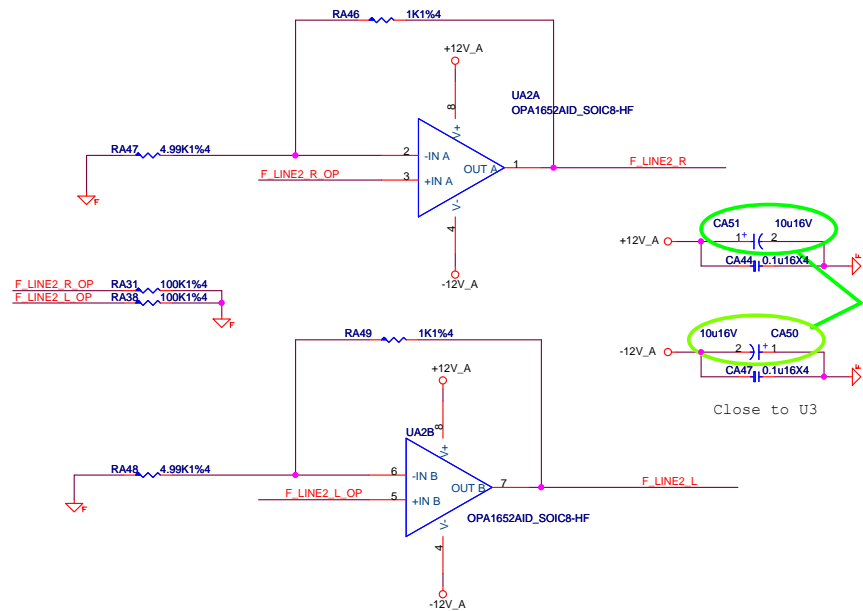
Vinafix.com

5	4	3	
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE			

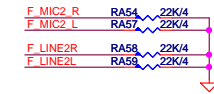
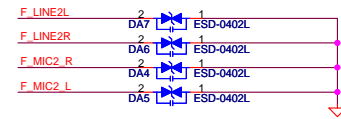


ALC1220

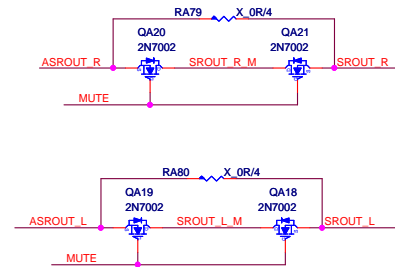
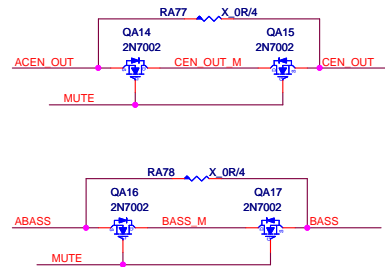
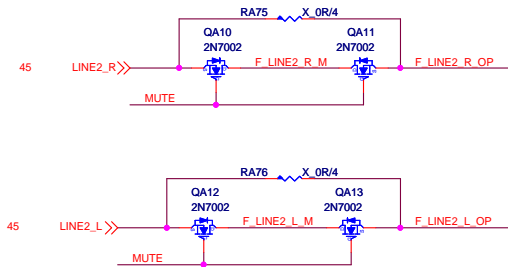
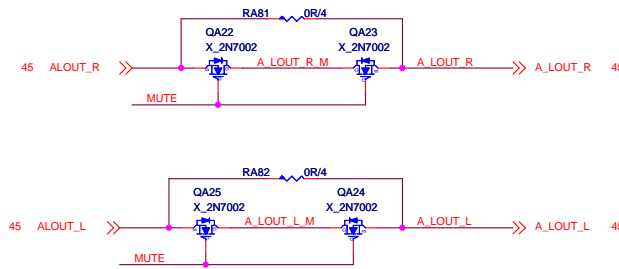
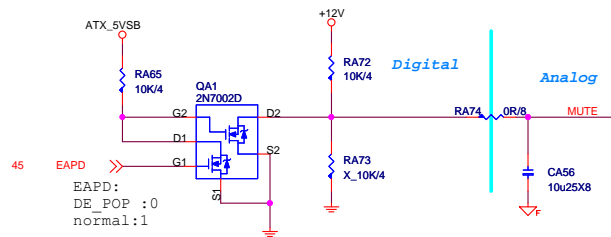




Close to Jack
ESD protect
D0G-2950500-S10
D0G-3010510-I05



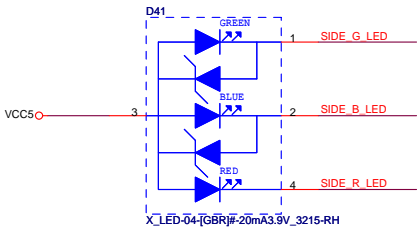
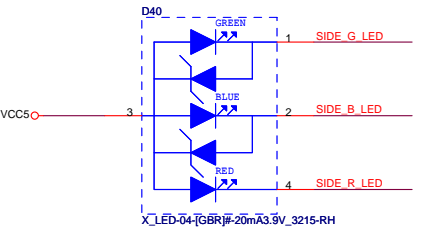
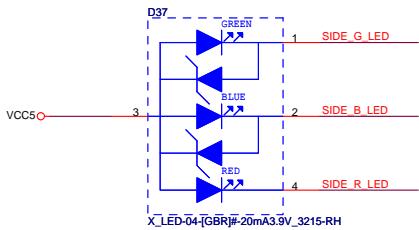
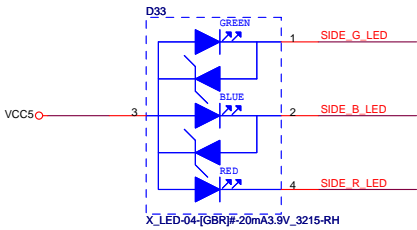
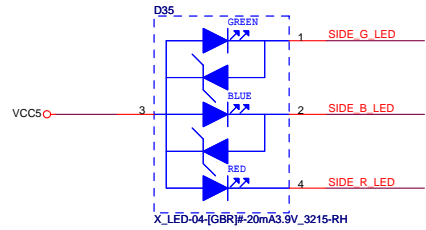
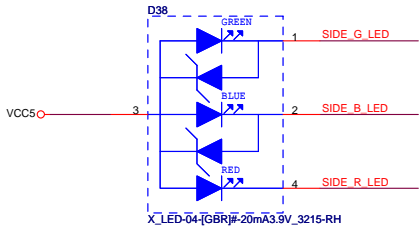
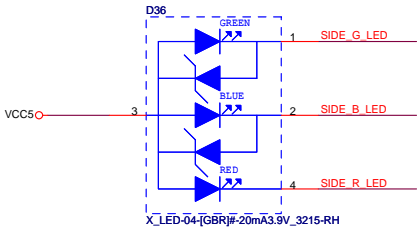
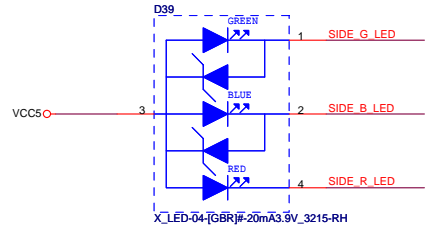
De-POP circuit



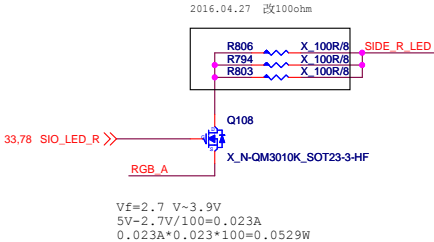
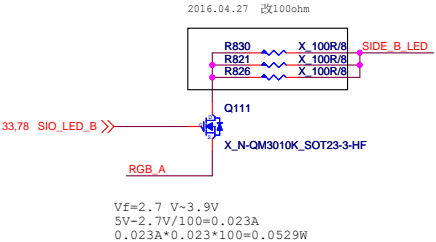
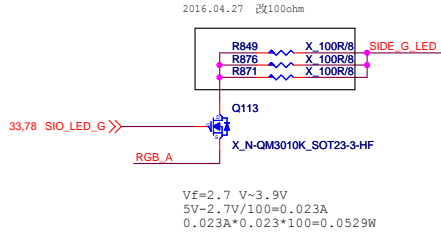
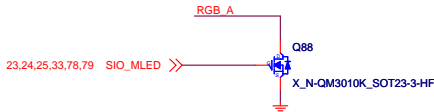
ASROUT_R 45
ASROUT_L 45
ACEN_OUT 45
ABASS 45
SROUT_L 45
SROUT_R 45
CEN_OUT 45
BASS 45

BOARD SIDE LED

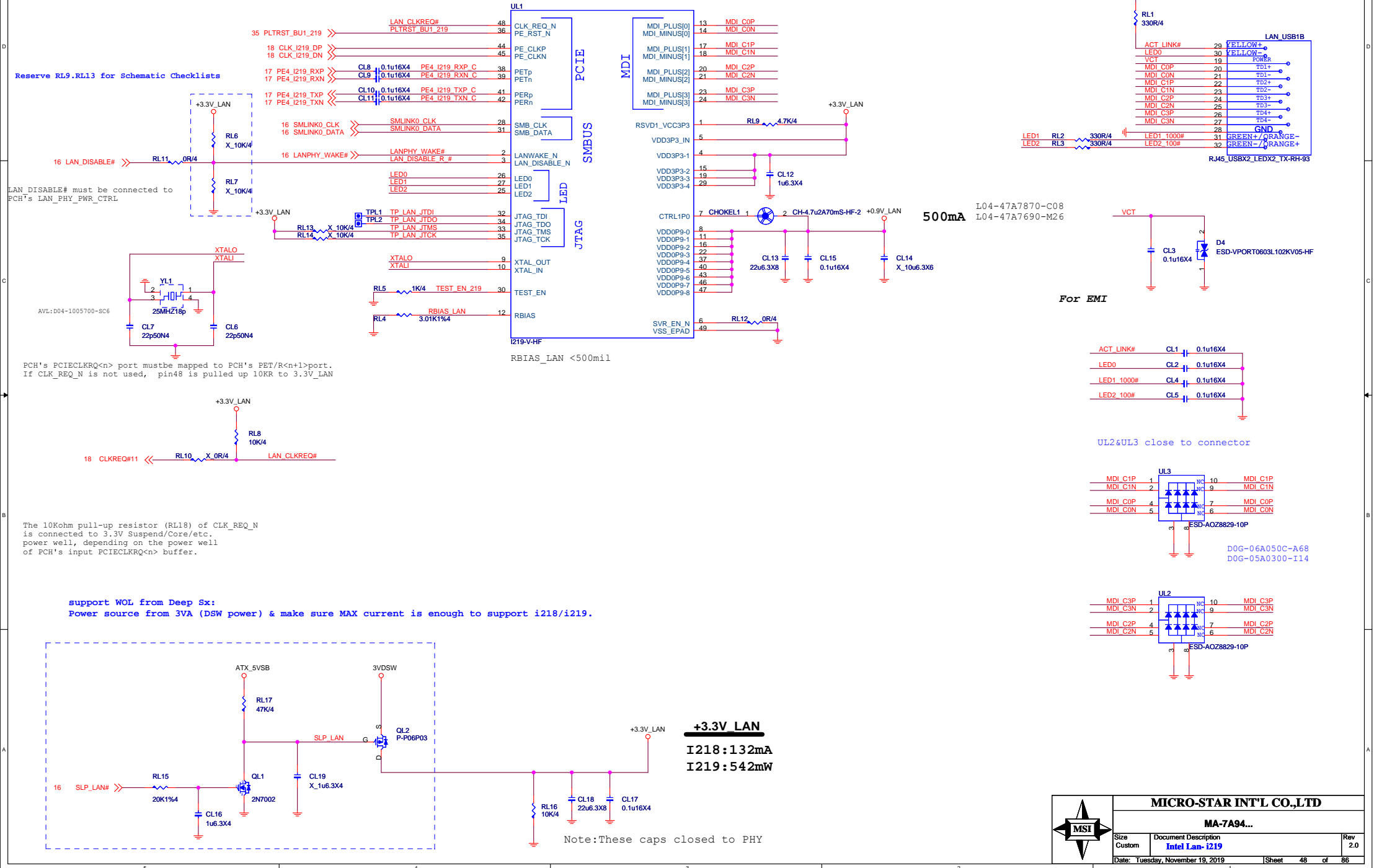
Audio moat is transparent and width 40mil



Vinafix.com



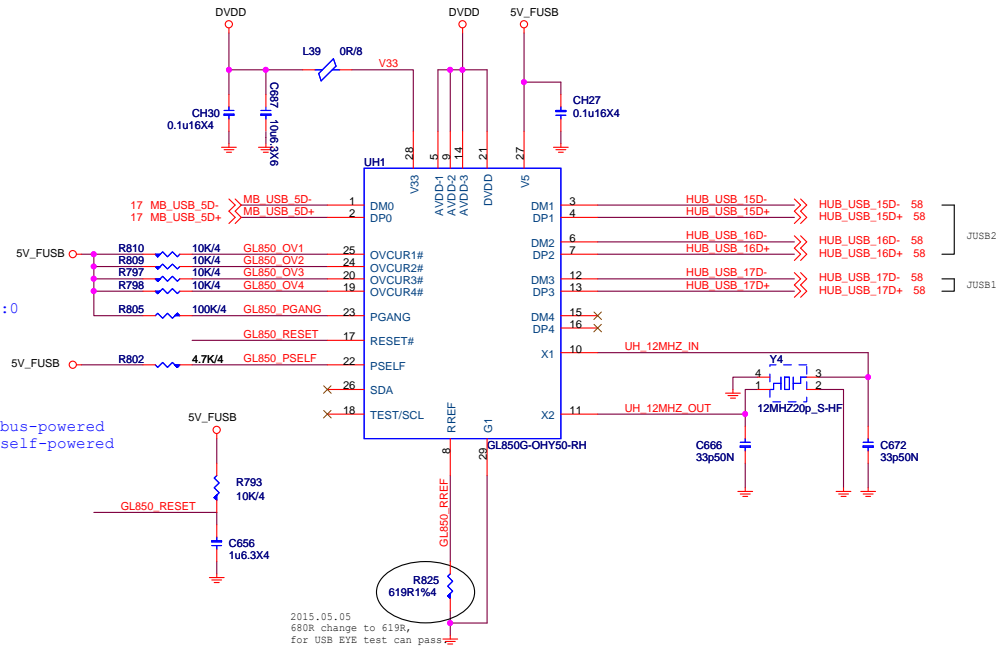
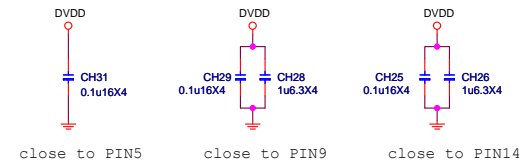
Intel I219V / I218V PHY



PIN23
Gang input:1
Individual input:0

PIN22
0: GL850G-50 is bus-powered
1: GL850G-50 is self-powered

Follow 7A49



2015.05.05
680R change to 619R,
for USB EYE test can pass

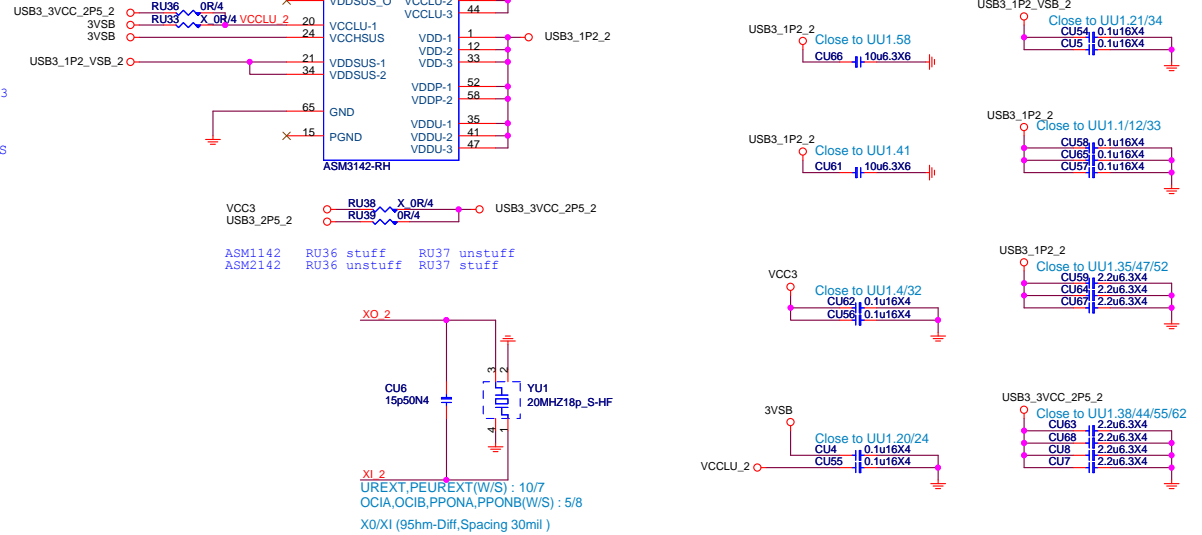
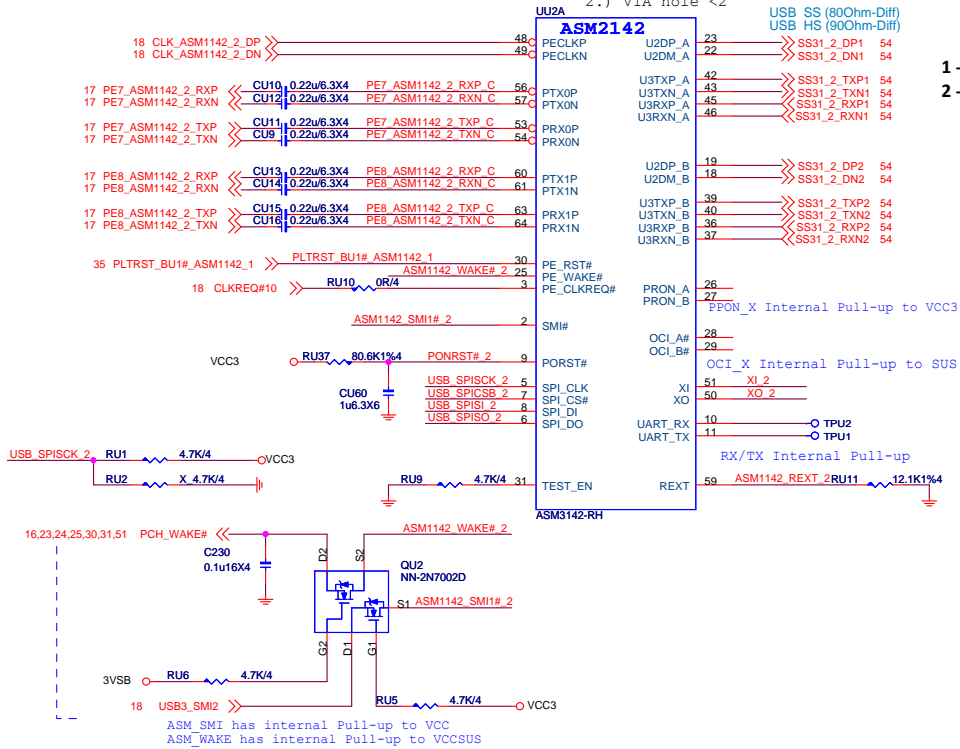
Vinafix.com

- Layout Guide:
- 1.) USB3.1 to Connector Total Length < 1.5"
 - 2.) VIA hole < 2

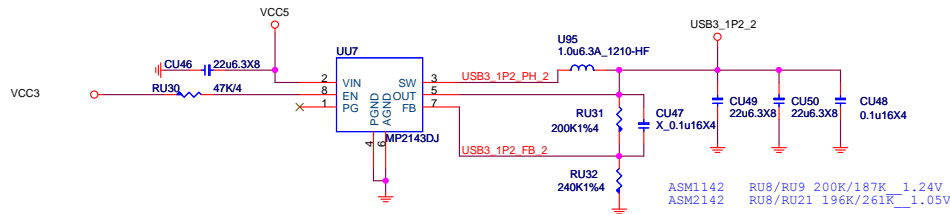
Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

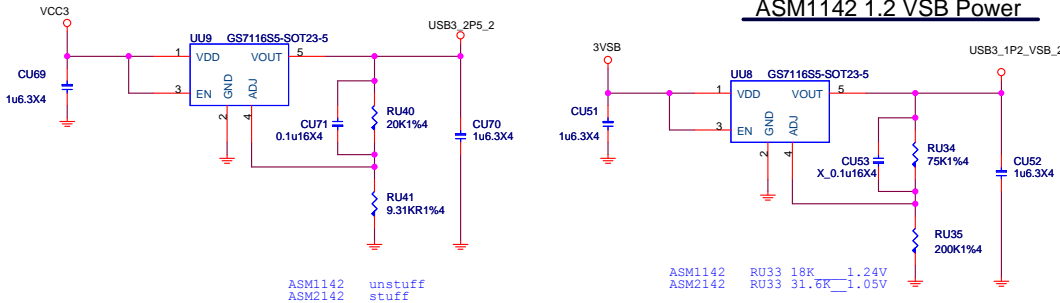
- 1 -> USB3.1-C
2 -> USB3.1-A



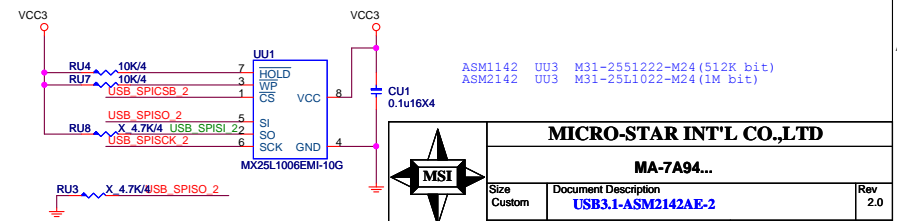
ASM1142 1.2 VCC Power



ASM1142 1.2 VSB Power



EEPROM



ASM1142 U03 M31-2551222-M24(512K bit)
ASM2142 U03 M31-25L1022-M24(1M bit)



MICRO-STAR INT'L CO.,LTD

MA-7A94...

Size	Document Description	Rev
Custom	USB3.1-ASM2142AE-2	2.0
Date:	Tuesday, November 19, 2019	Sheet 50 of 86

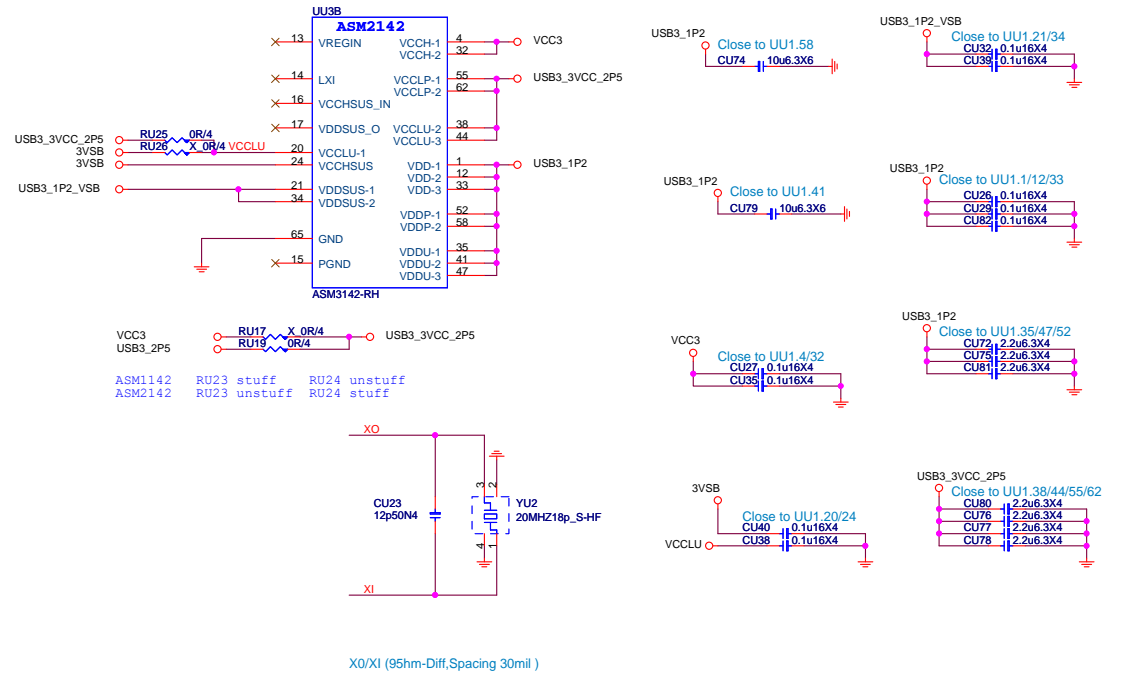
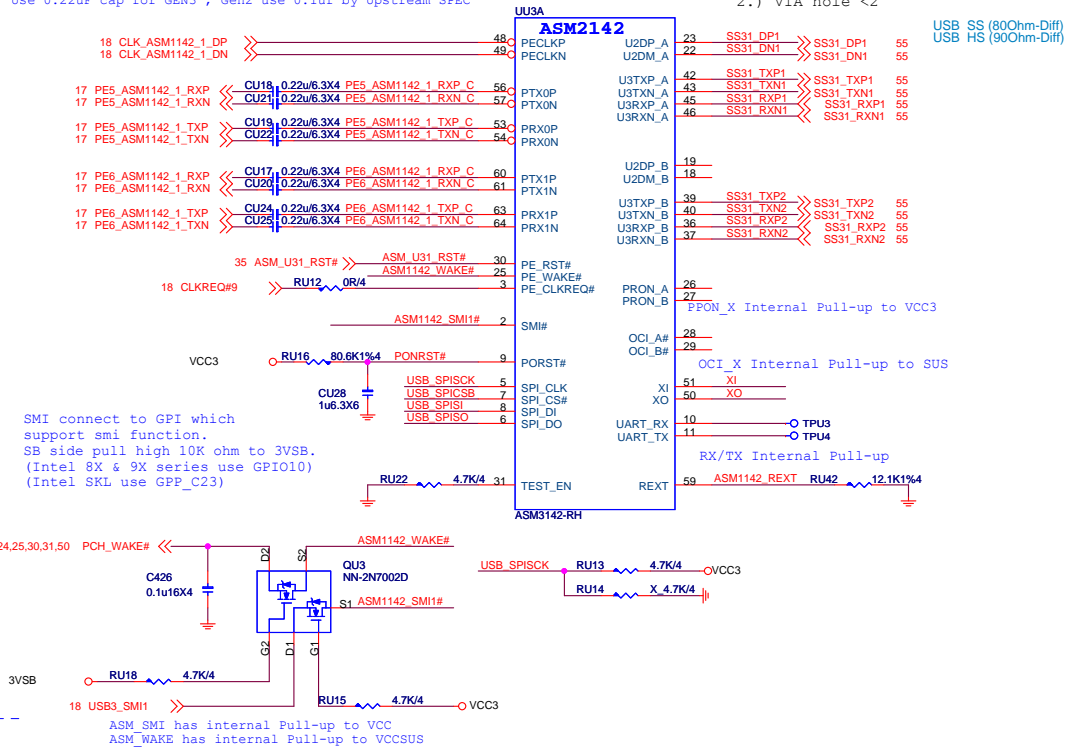
Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC

Layout Guide:

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

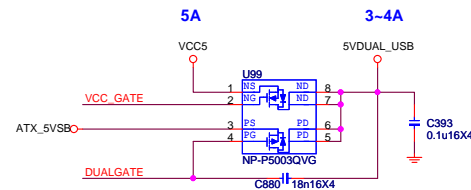
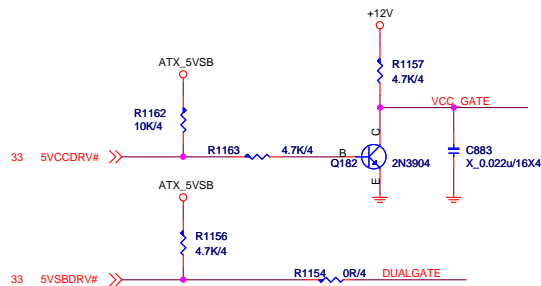


F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

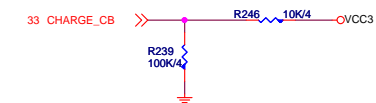
F75504 PM request Remove 0407 mail

Vinafix.com

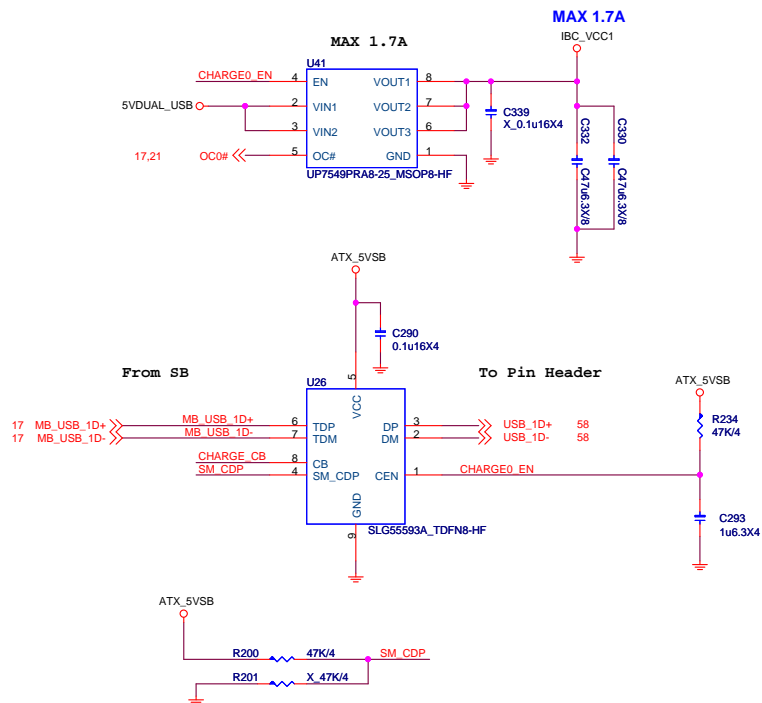
5VDUAL_USB



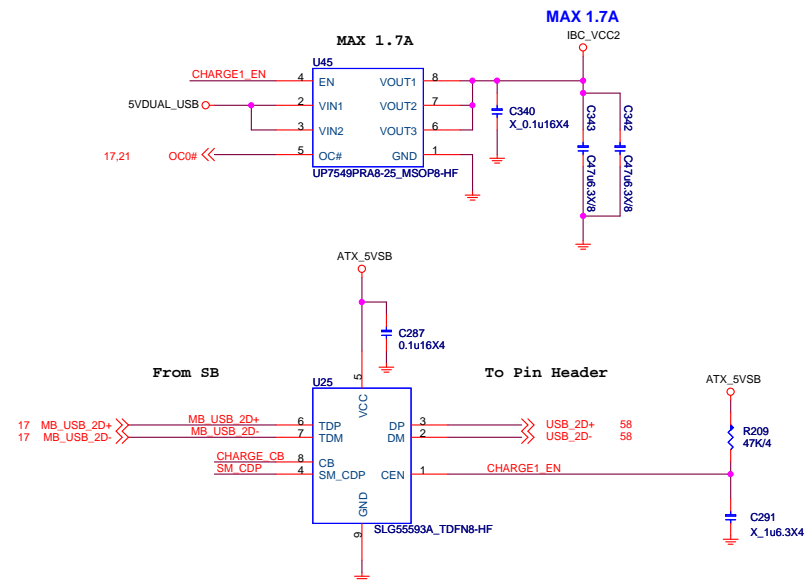
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging

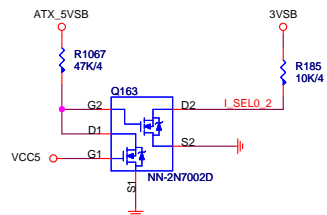


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB CHARGE_SLG55593A	2.0
Date: Tuesday, November 19, 2019	Sheet 53 of 86	

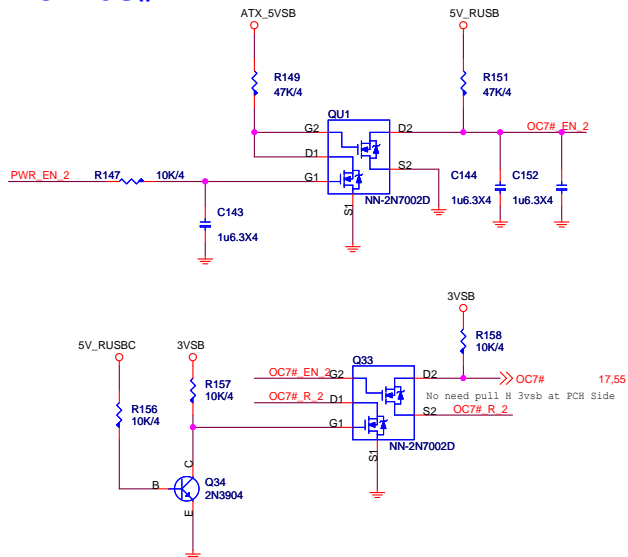
Current Mode



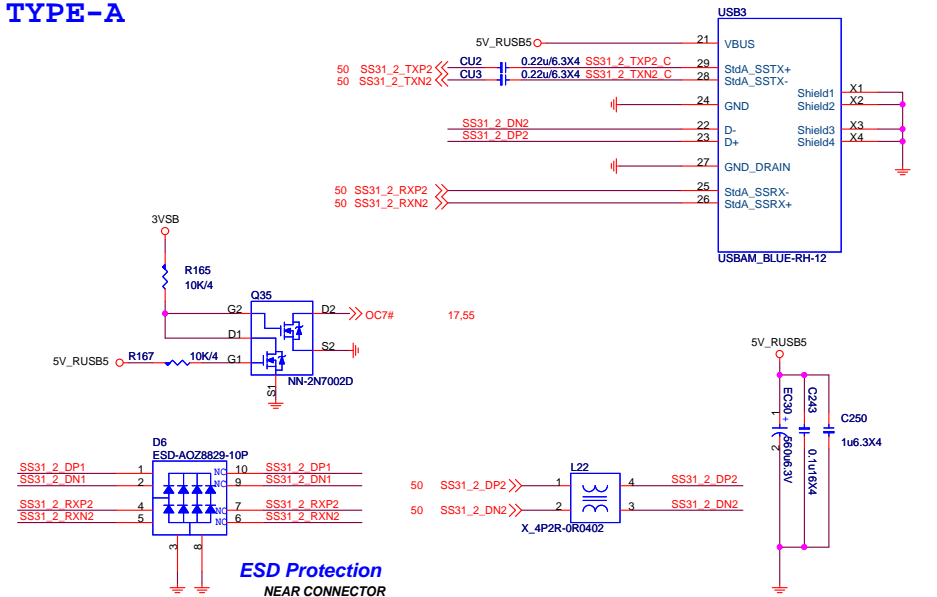
0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

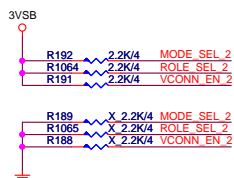
VBUS OC#



TYPE-A



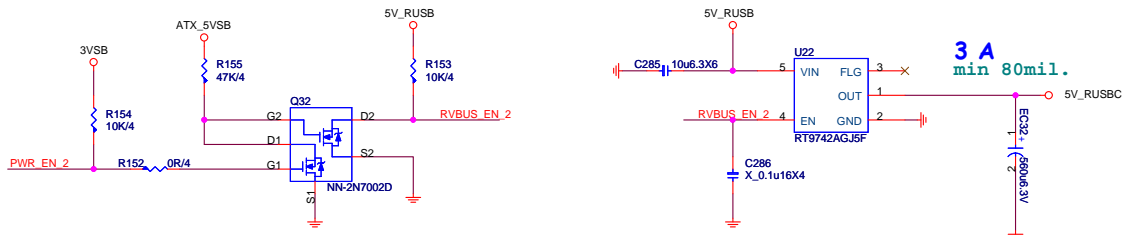
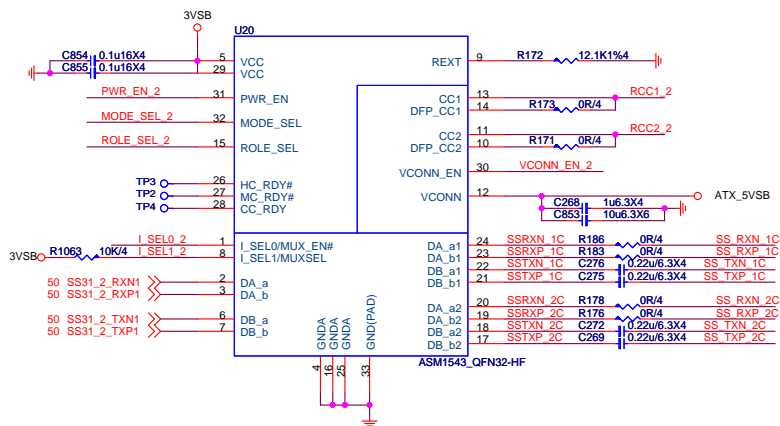
USB Type-C MUX with Configuration Channel (CC)



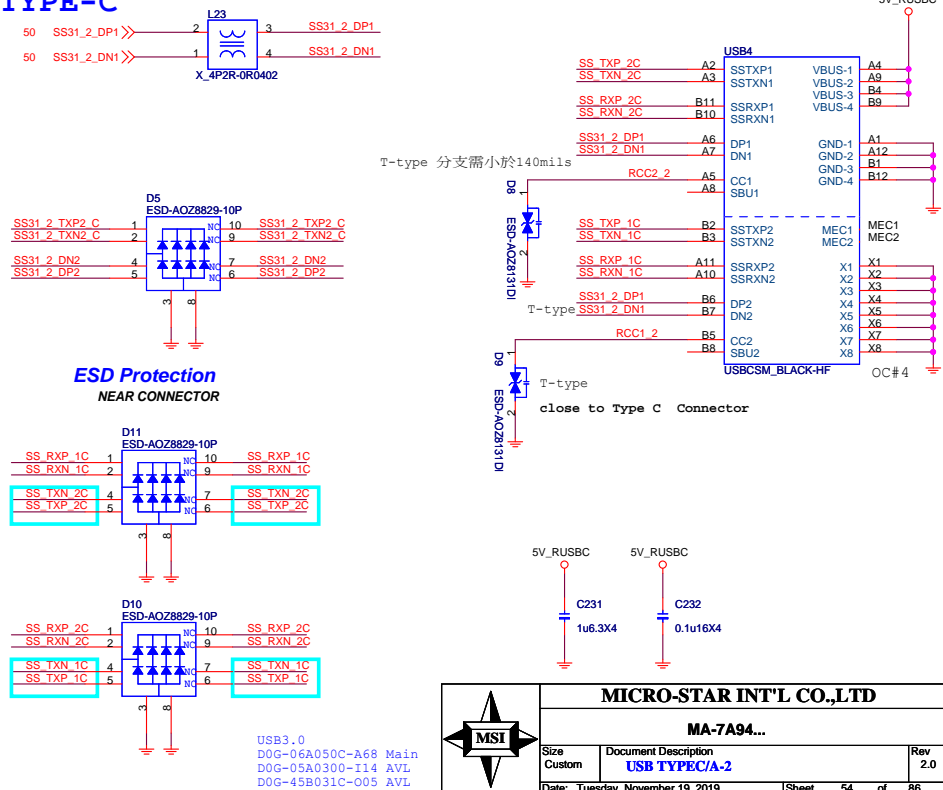
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFF role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable



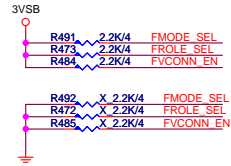
TYPE-C



MICRO-STAR INT'L CO.,LTD			
MA-7A94...			
Size	Document Description	Rev	
Custom	USB TYPE-C/A-2	2.0	
Date:	Tuesday, November 19, 2019	Sheet	54 of 86

USB 3.1-Type-C

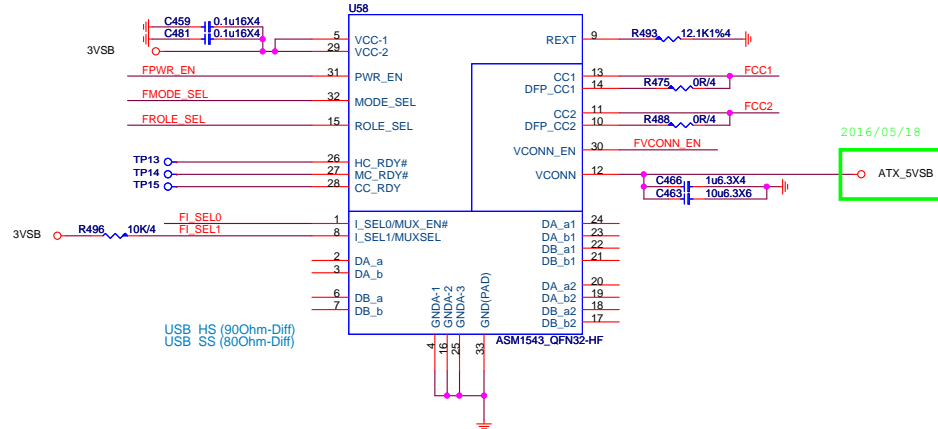
USB Type-C MUX with Configuration Channel (CC)



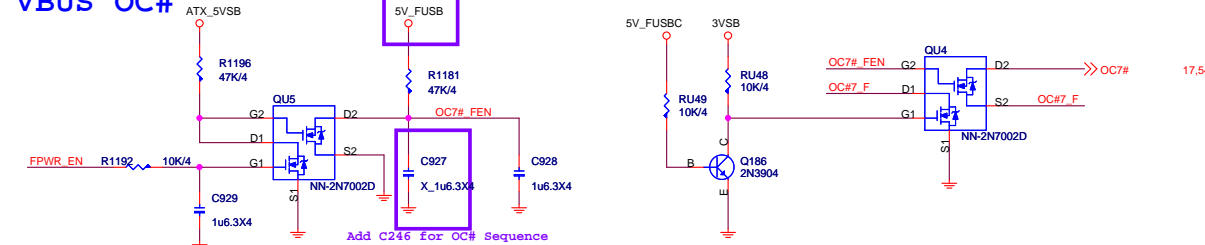
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

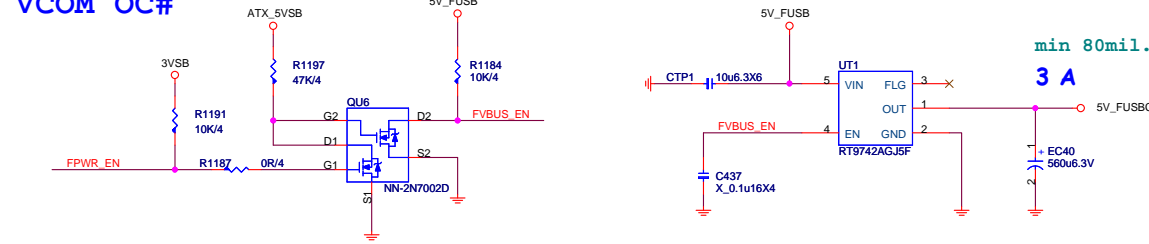
VCONN_EN	
1	enable
0	disable



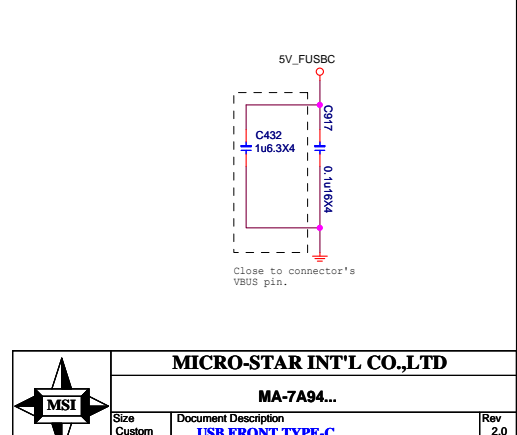
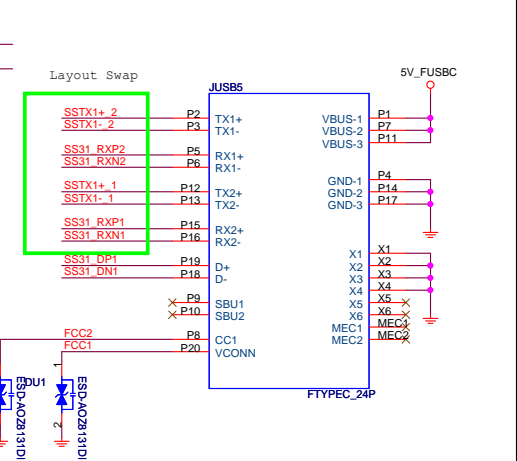
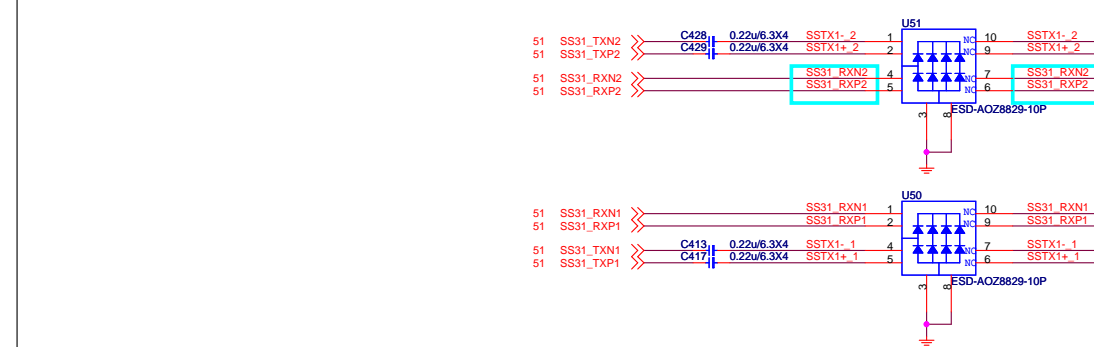
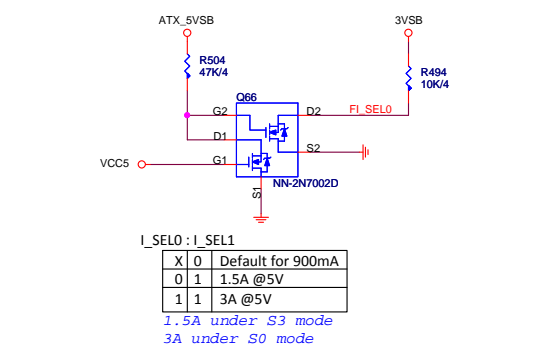
VBUS OC#



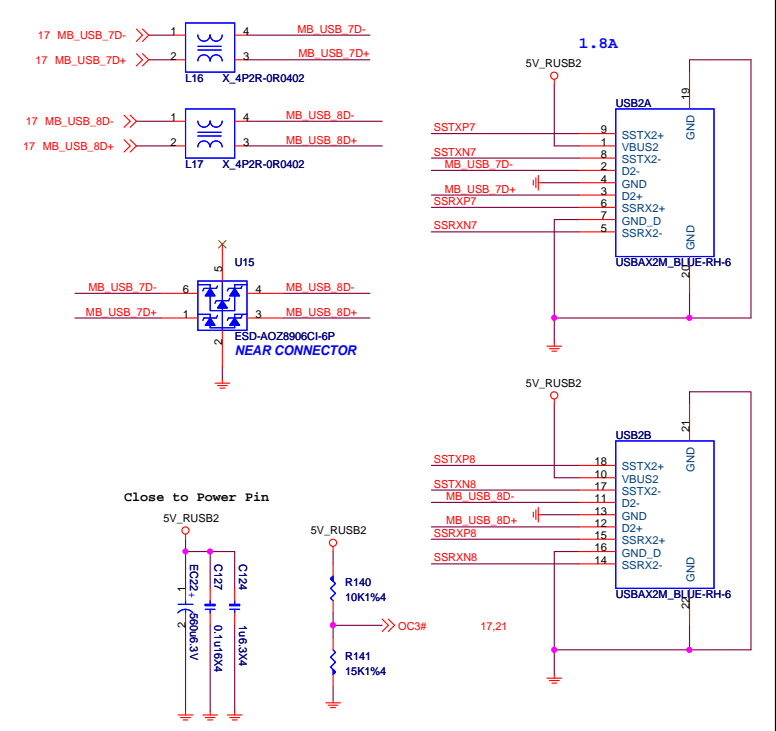
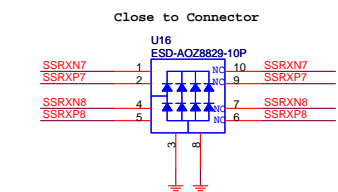
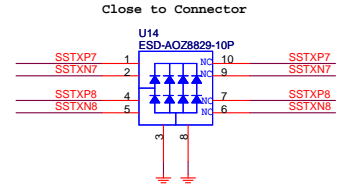
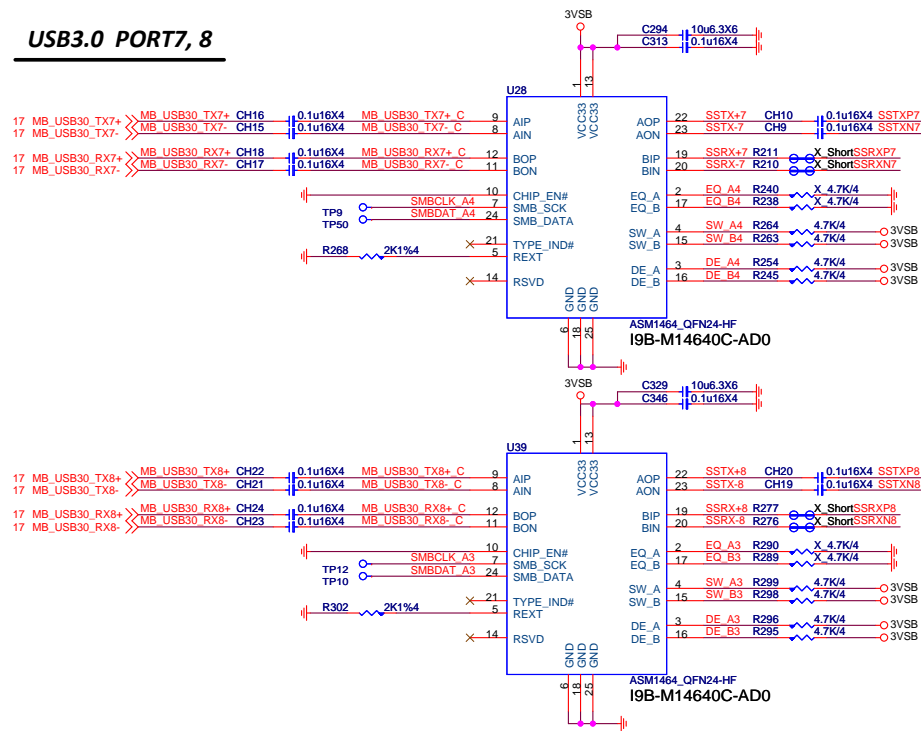
VCOM OC#



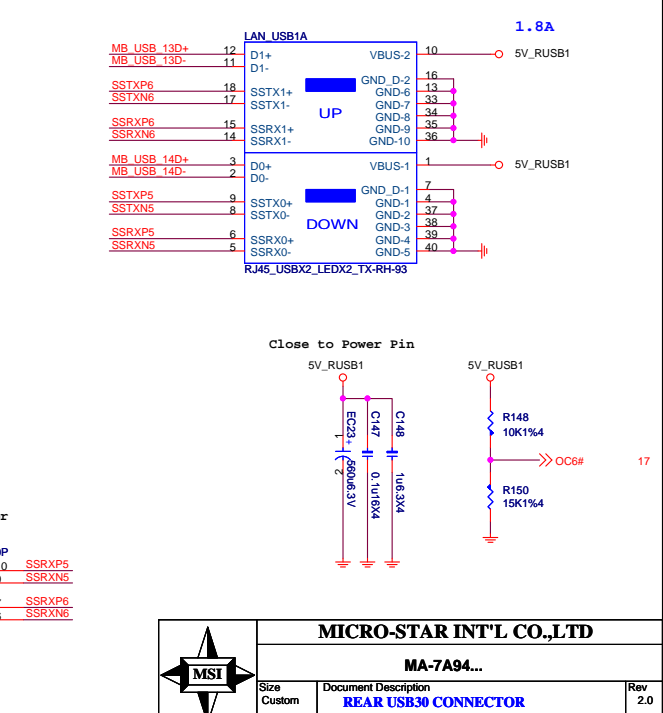
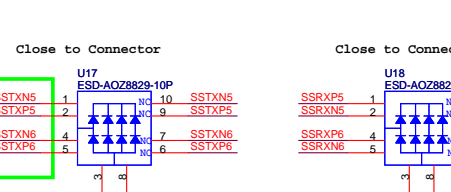
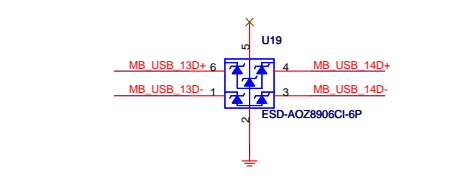
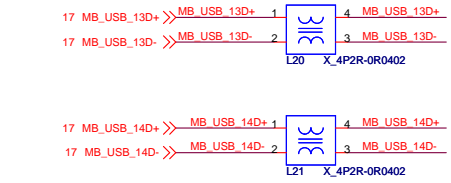
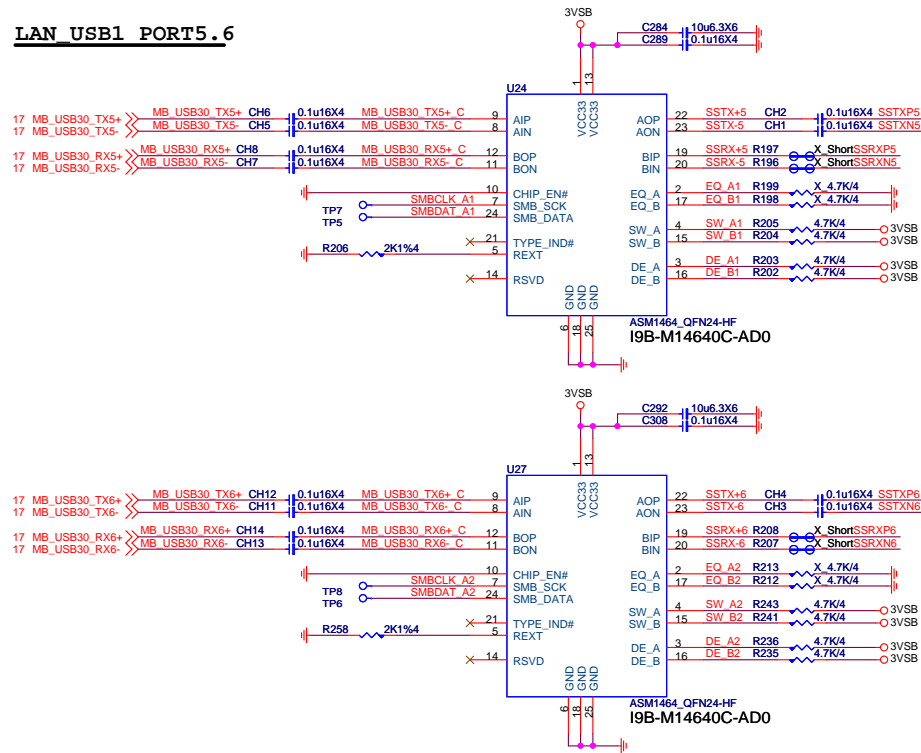
Current Mode



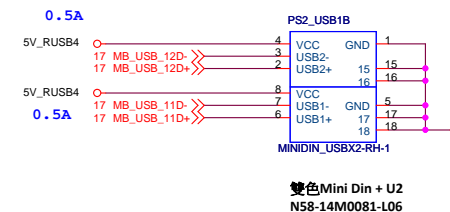
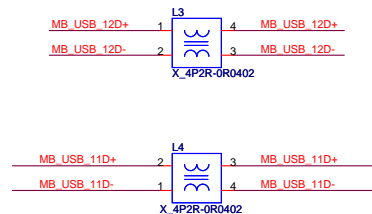
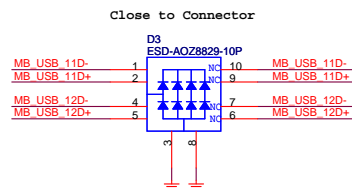
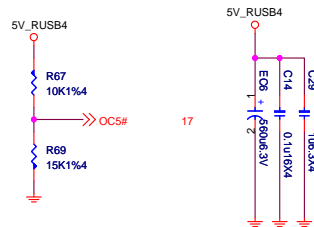
USB3.0 PORT7, 8



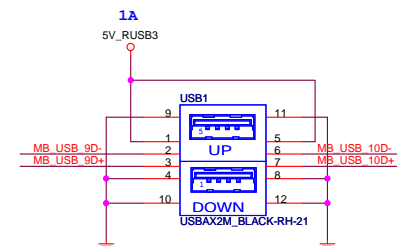
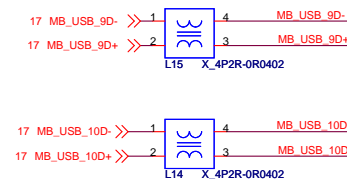
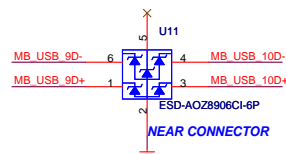
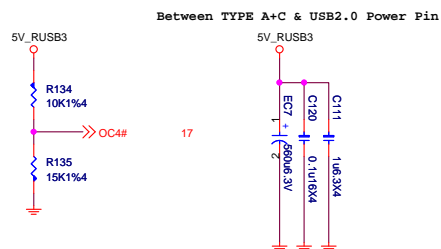
LAN USB1 PORT5.6



PS2_USB1



USB2.0 PORT9, 10

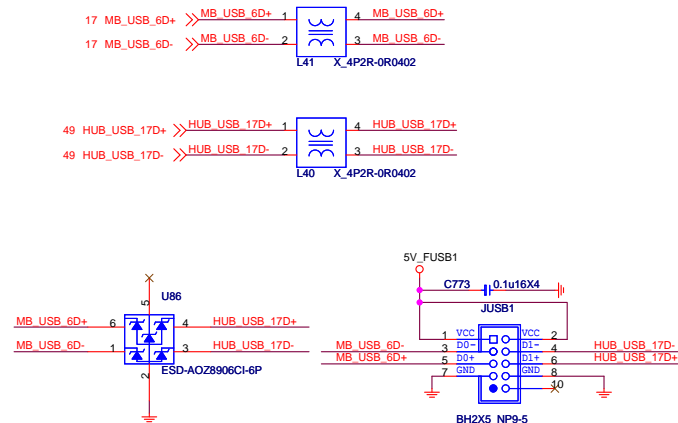


MICRO-STAR INT'L CO.,LTD

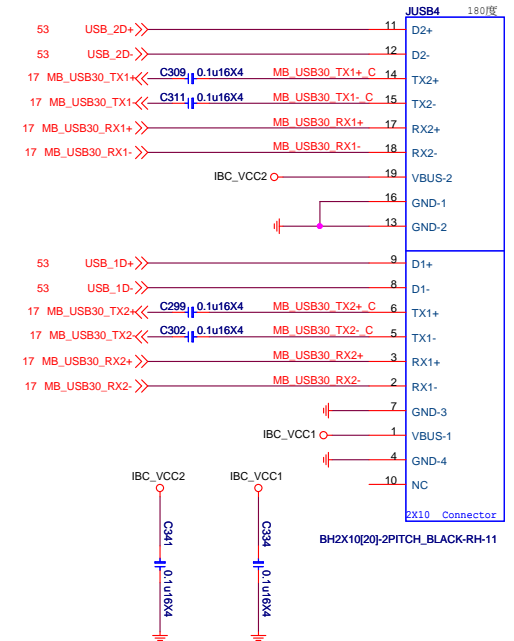
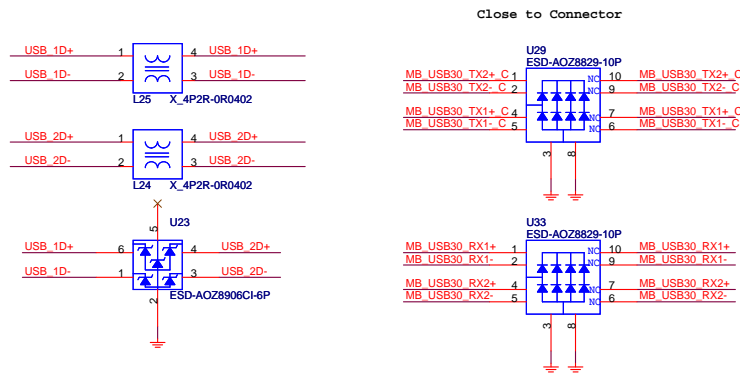
MA-7A94...

Size	Document Description	Rev
Custom	REAR USB20 CONNECTOR	2.0
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FRONT USB PORT 6. HUB PORT 17

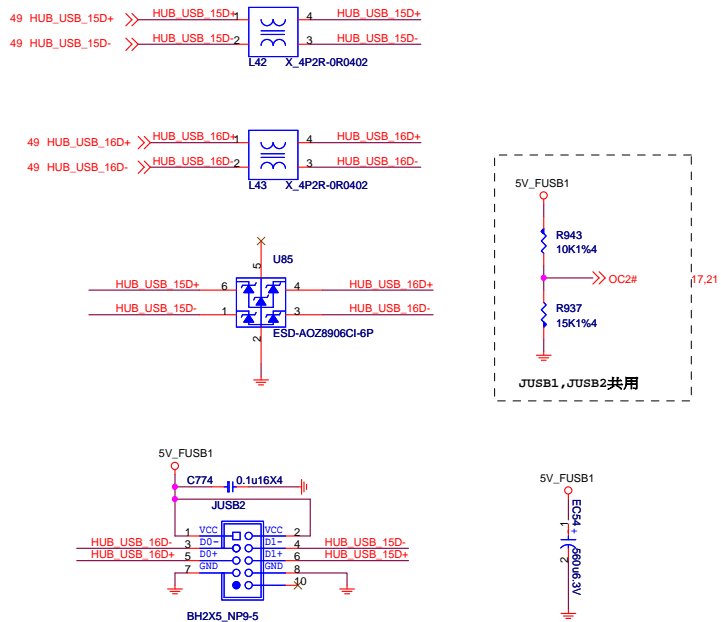


FRONT USB PORT 1,2

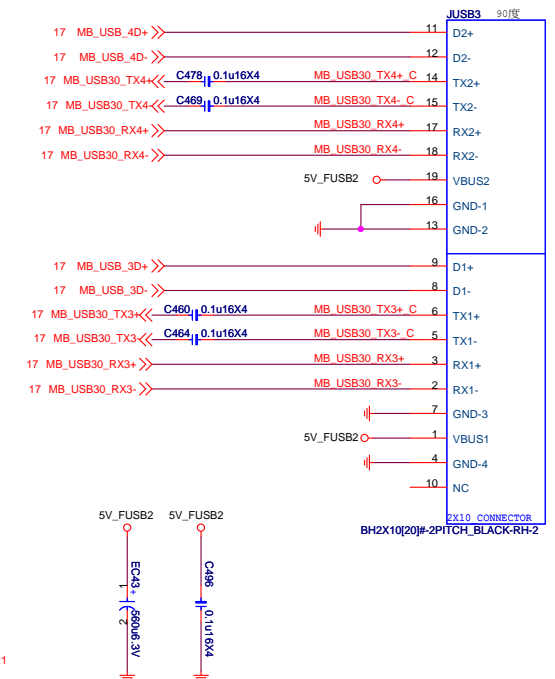
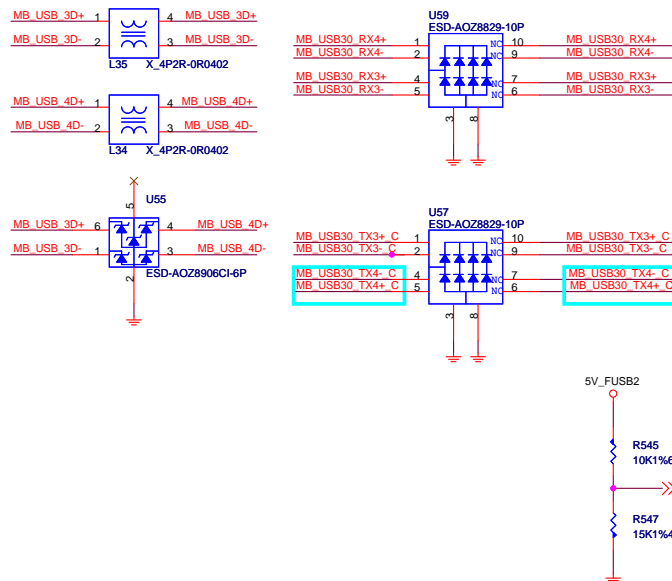


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FRONT USB HUB PORT 15,16

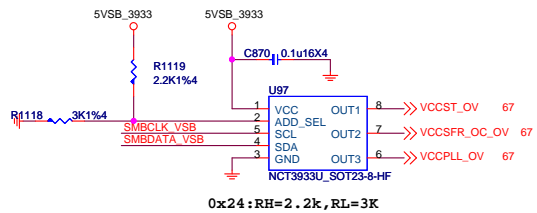


FRONT USB PORT 3,4

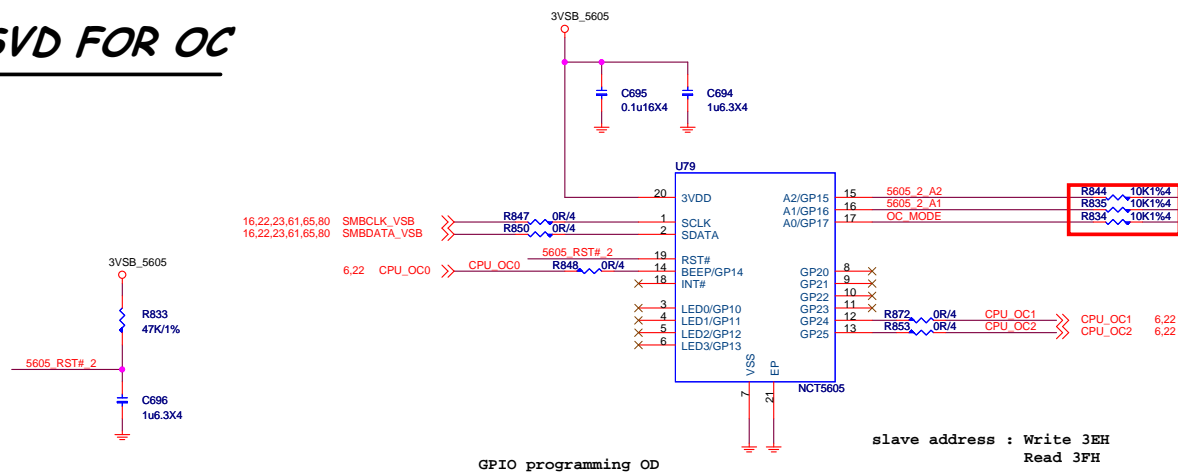
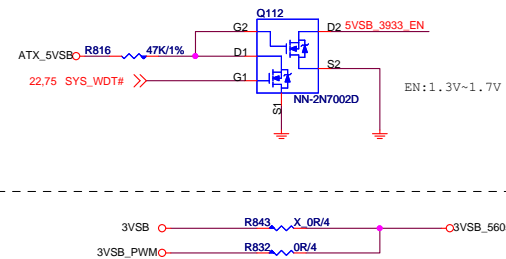
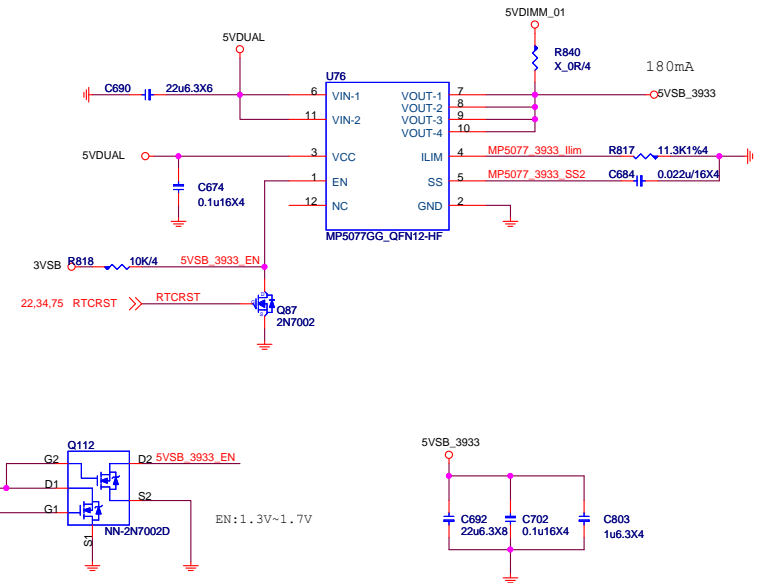


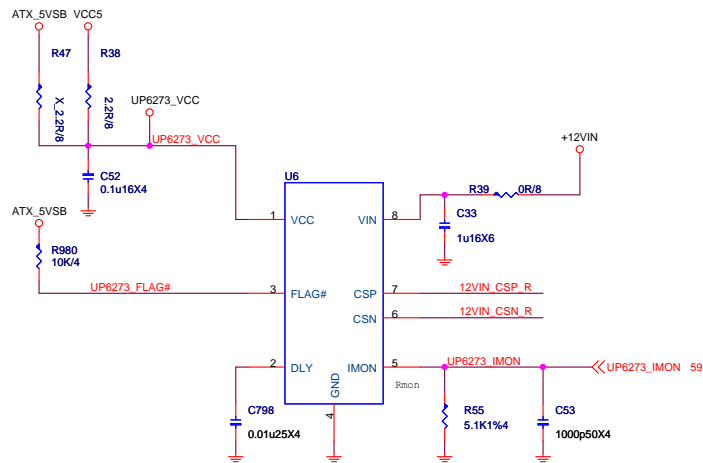
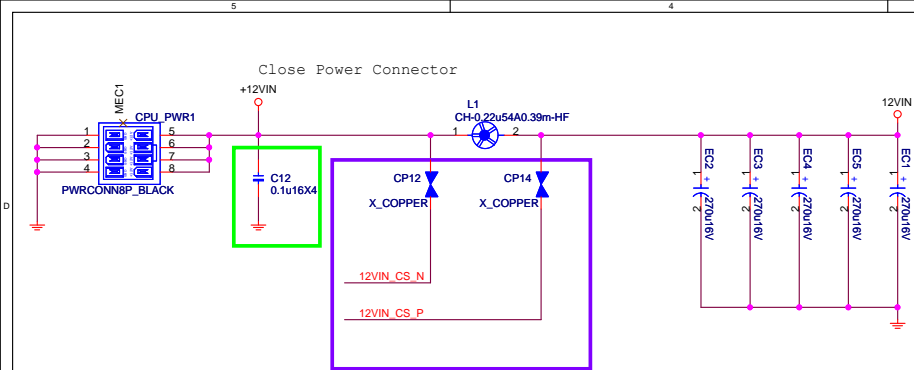
MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	Rear/Front USB2.0	2.0	
Date:	Tuesday, November 19, 2019	Sheet	58 of 86

RSVD FOR OC



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%





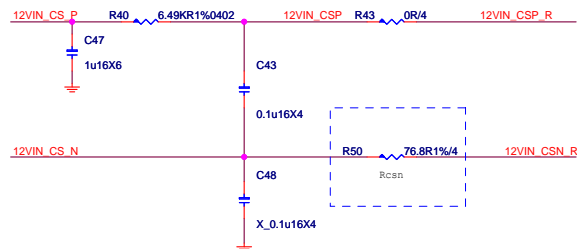
UP6273AMT8_TSOP23-8-HF

$I_{in} = (V_{mon} * R_{csn}) / (R_{mon} * R_{dc})$
 $V_{mon} = 1.2$
 can change OCP trigger level by R_{csn} and R_{mon}

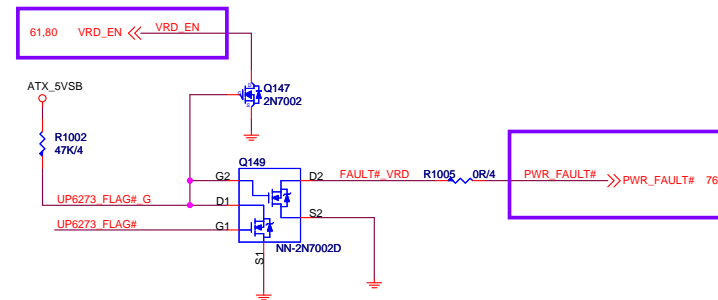
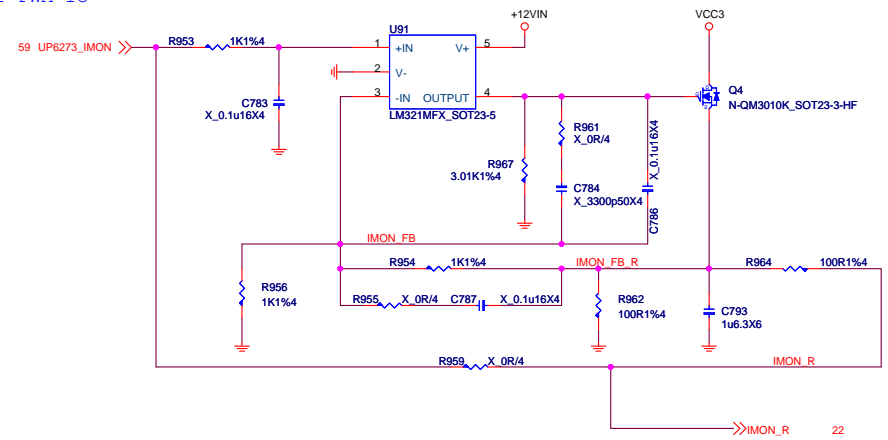
$I_{in} * R_{dc} * R_{mon} / R_{csn} > V_{mon}$
 $48 * 0.39m * 5.1K / 76.8 = 1.243$

$I_{mon} * R_{csn} / R_{dc} = I_{in}$
 $10u * 76.8 / 0.39m = 1.969A$

—階2A
 $R_{mon} = 5.1K\Omega$
 $R_{csn} = 0.0768K\Omega$
 $DCR = 0.39m\Omega$
 $V_{mon} = 1.2V$
 $I_{ocp} = 48A$



Near PWM IC

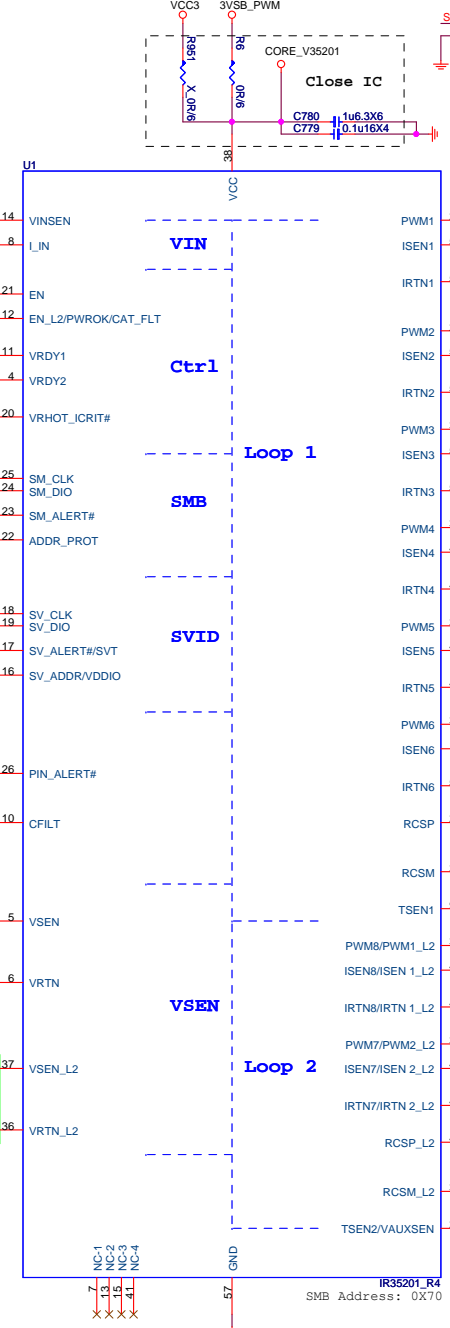
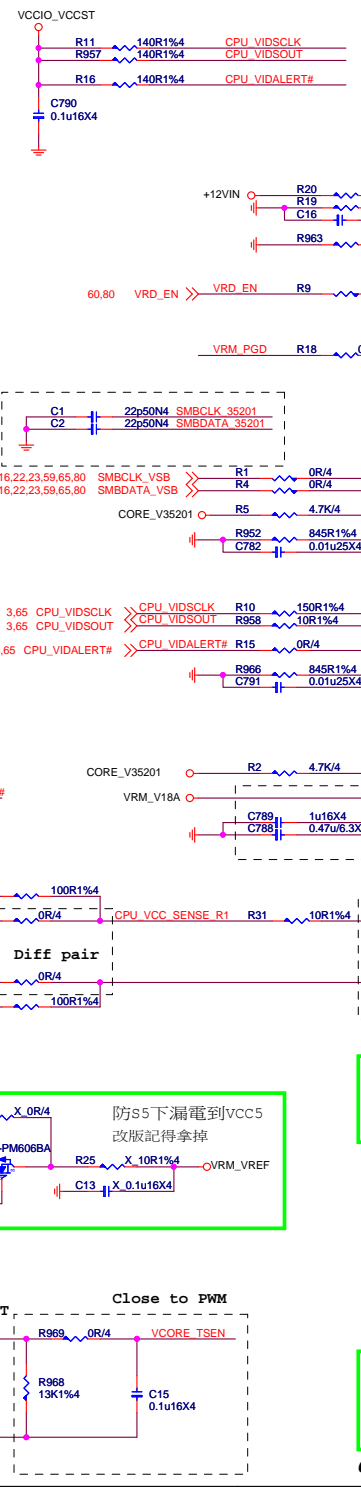
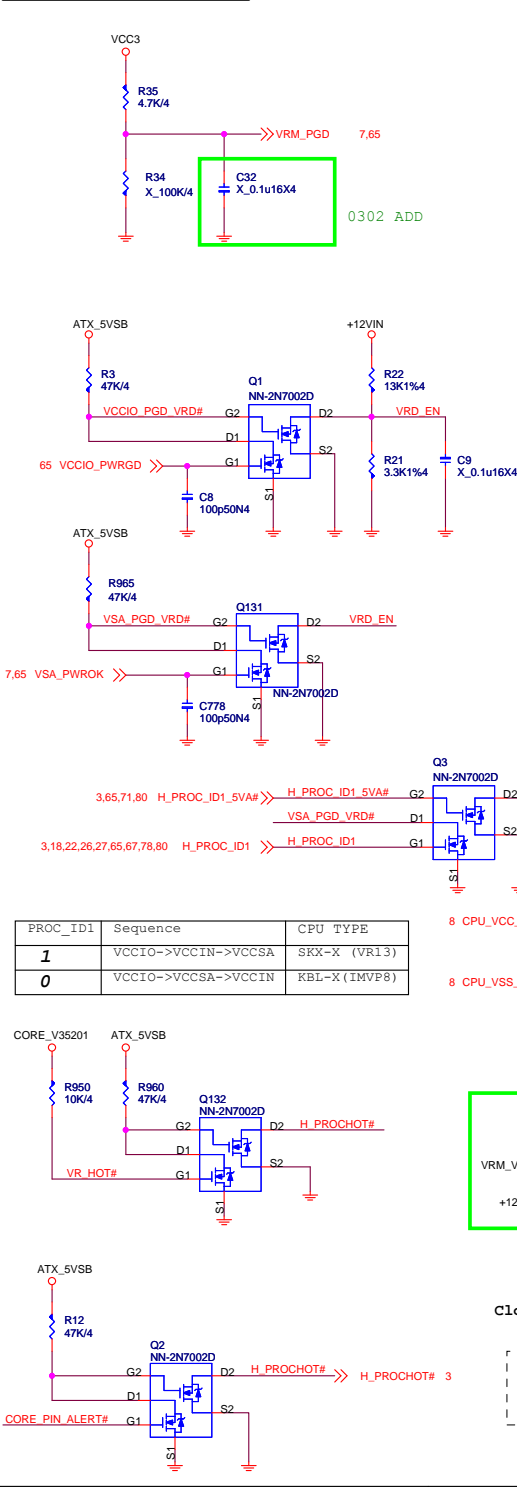


MICRO-STAR INT'L CO.,LTD

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Custom	12VIN SENSE RT9553	2.0
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VRMPWRGD LEVEL SHIFT



Vcore: ICC Max 100A
LL: 1.0 mohm
OCP: 320A
VSA: ICC Max 15A
OCP: 40A

teknisi indonesia

VCORE_ISEN6_R

VCORE_ISEN6_R

VCORE_ISEN8_R

VCORE_ISEN7_R

VCORE_ISEN7_R

VCORE_ISEN7_R

VCORE_ISEN7_R

VCORE_ISEN7_R

PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X (IMVP8)

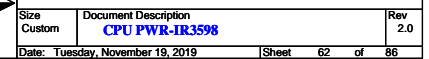
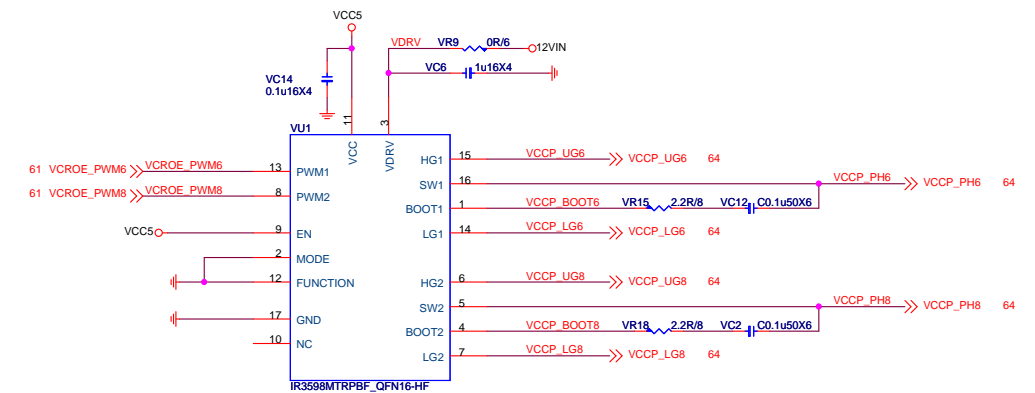
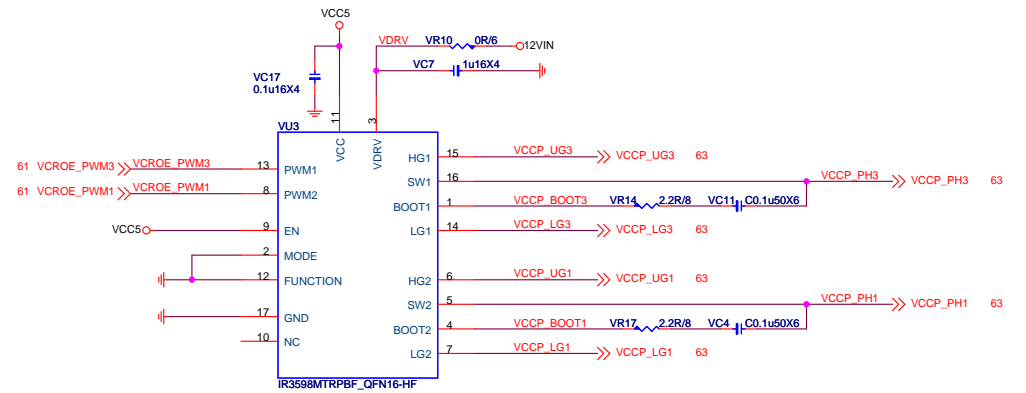
Default	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

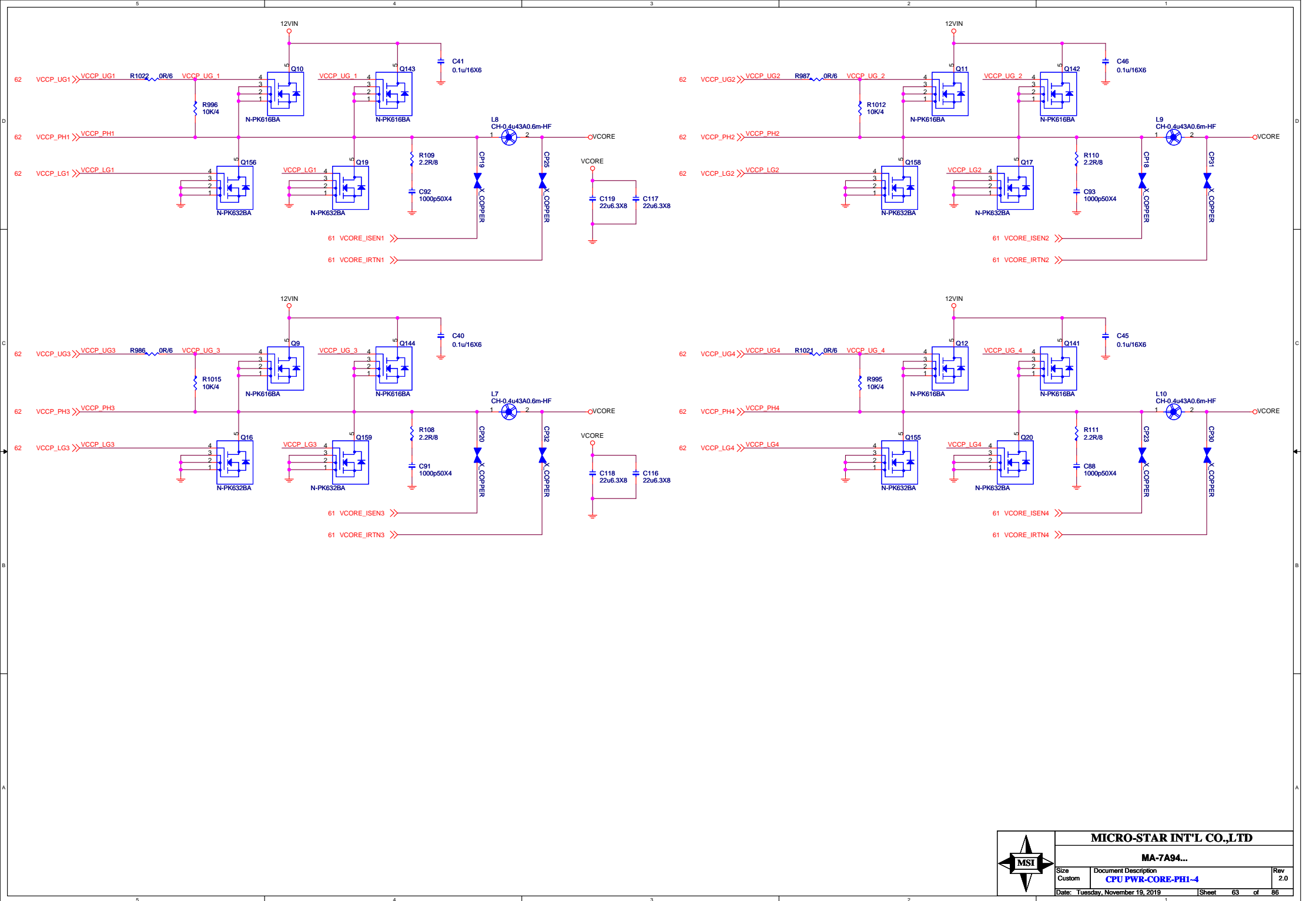
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description CPU PWR-IR35201	Rev 2.0
Date: Tuesday, November 19, 2019	Sheet 61	of 86

dummy load for SEN pin 漏電

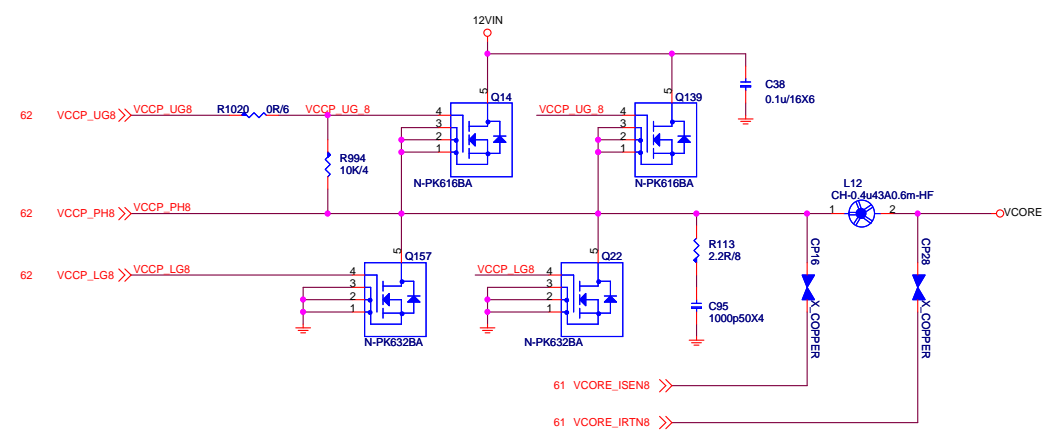
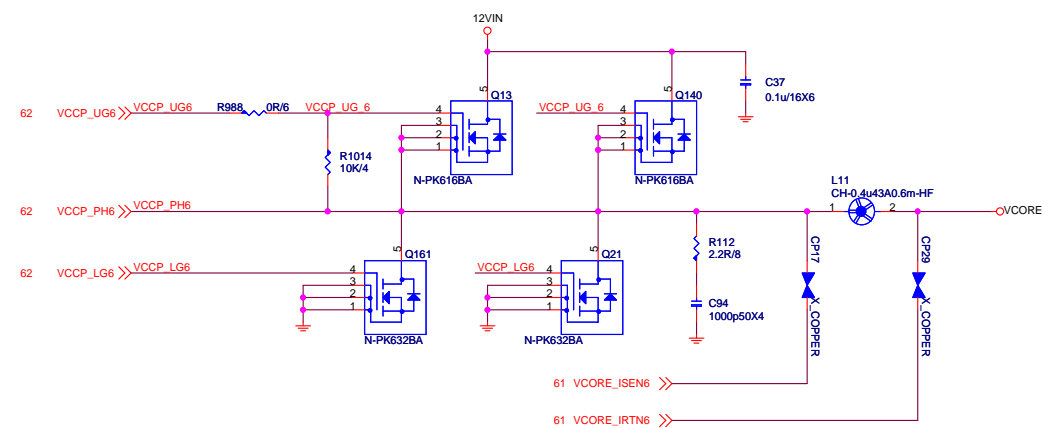




MICRO-STAR INT'L CO.,LTD

MA-7A94...

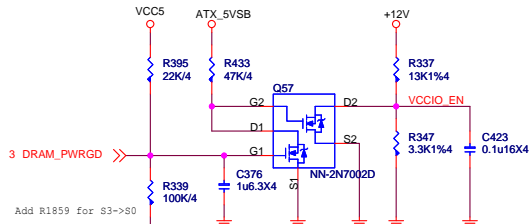
Size	Document Description	Rev
Custom	CPU PWR-CORE-PH1-4	2.0
Date: Tuesday, November 19, 2019		Sheet 63 of 86



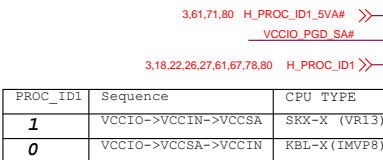
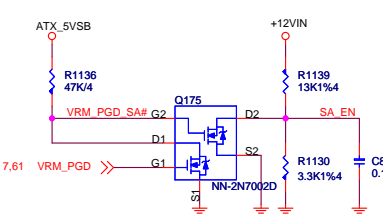
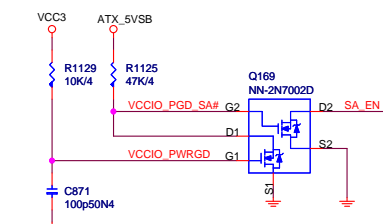
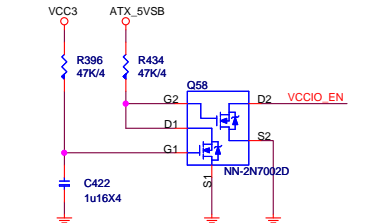
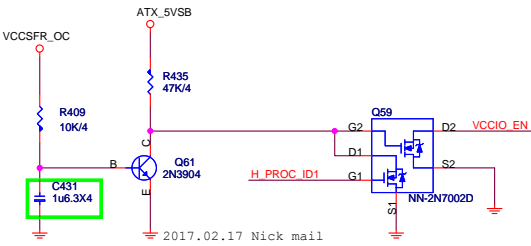
MA-7A94...

Size Custom	Document Description CPU PWR-CORE-PH5~8	Rev 2.0
Date: Tuesday, November 19, 2019		Sheet 64 of 86

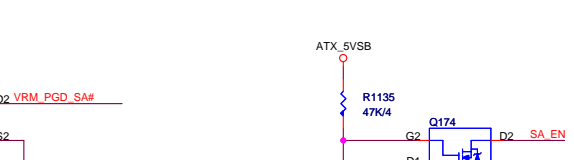
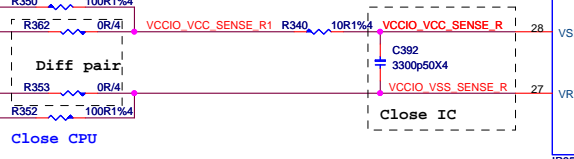
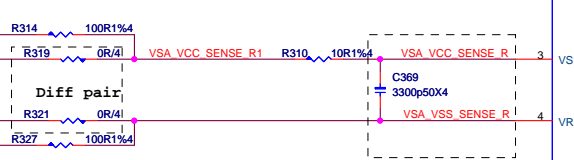
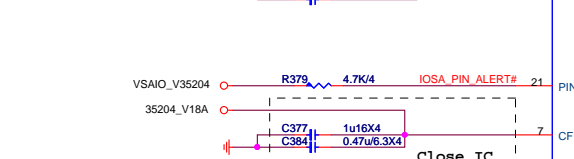
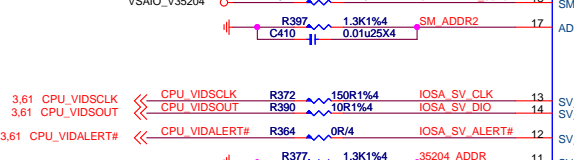
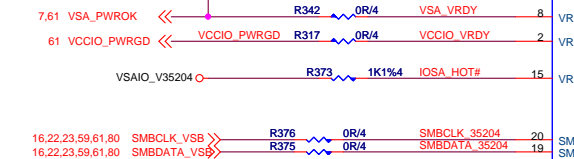
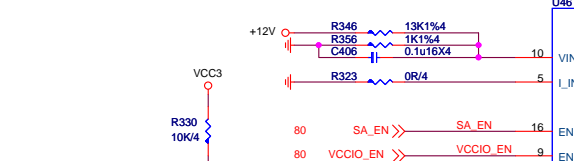
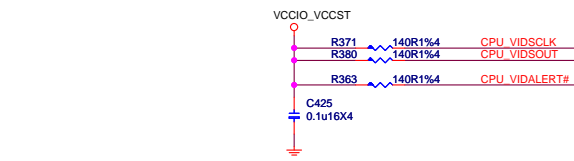
VCCIO_PWRGD LEVEL SHIFT



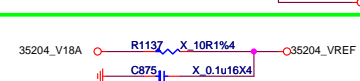
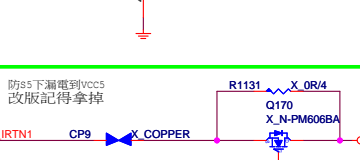
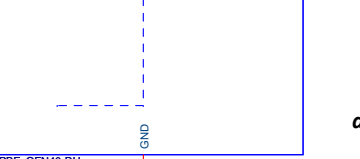
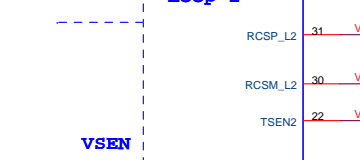
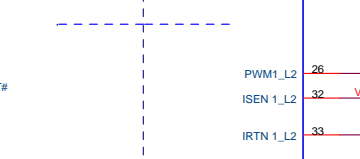
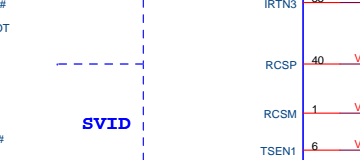
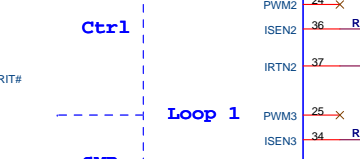
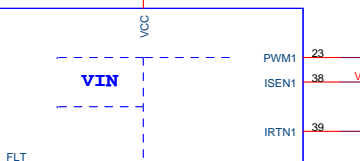
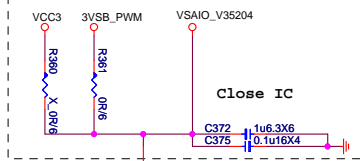
RSVD For KBL-X VCCIO Sequence



PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X (IMVP8)



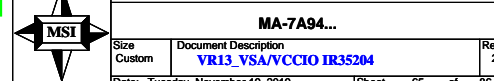
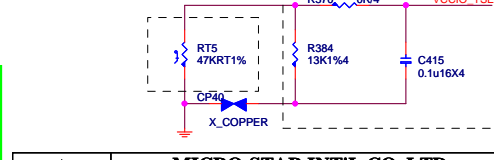
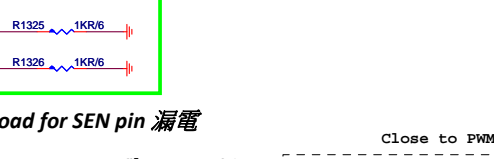
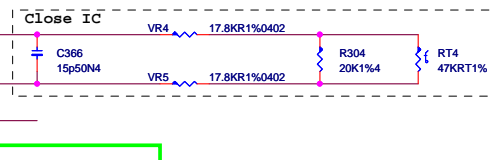
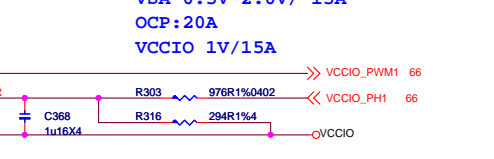
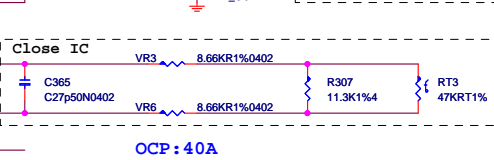
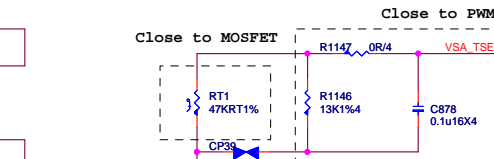
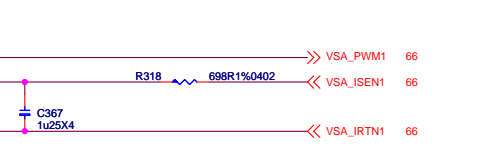
106.07.20 Ryan mail
防止進入S3時, SA_EN掉電未完全時, PWRSE偷打



106.07.20 Ryan mail
防止進入S3時, SA_EN掉電未完全時, PWRSE偷打

CPU ID CFG

PROC_ID1	PROC_ID0	CPU TYPE
0	0	future CPU(IMVP9)
0	1	KBL-X(IMVP8)
1	0	future CPU
1	1	SKX-X (VR13)



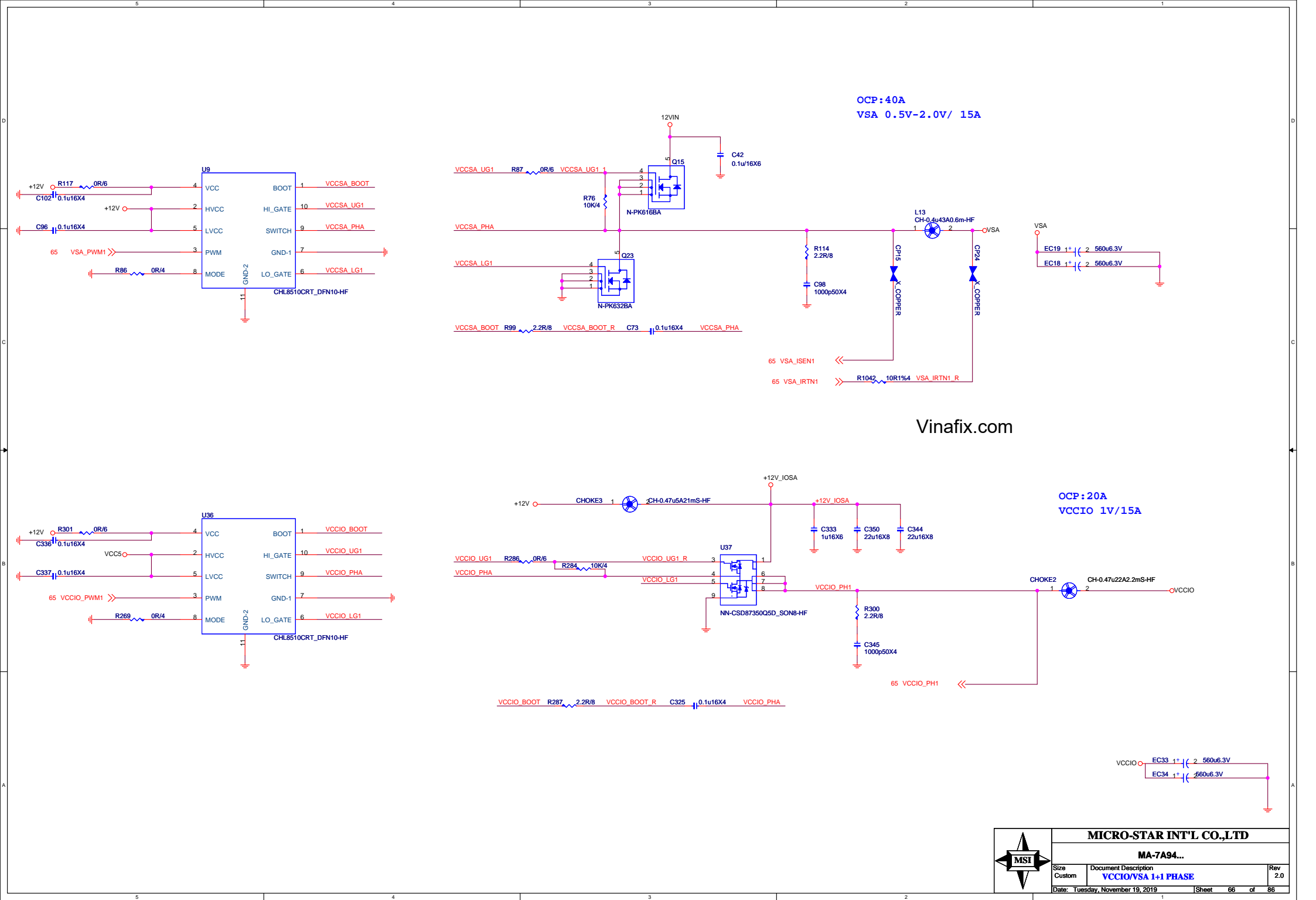
106.07.20 Ryan mail
防止進入S3時, SA_EN掉電未完全時, PWRSE偷打

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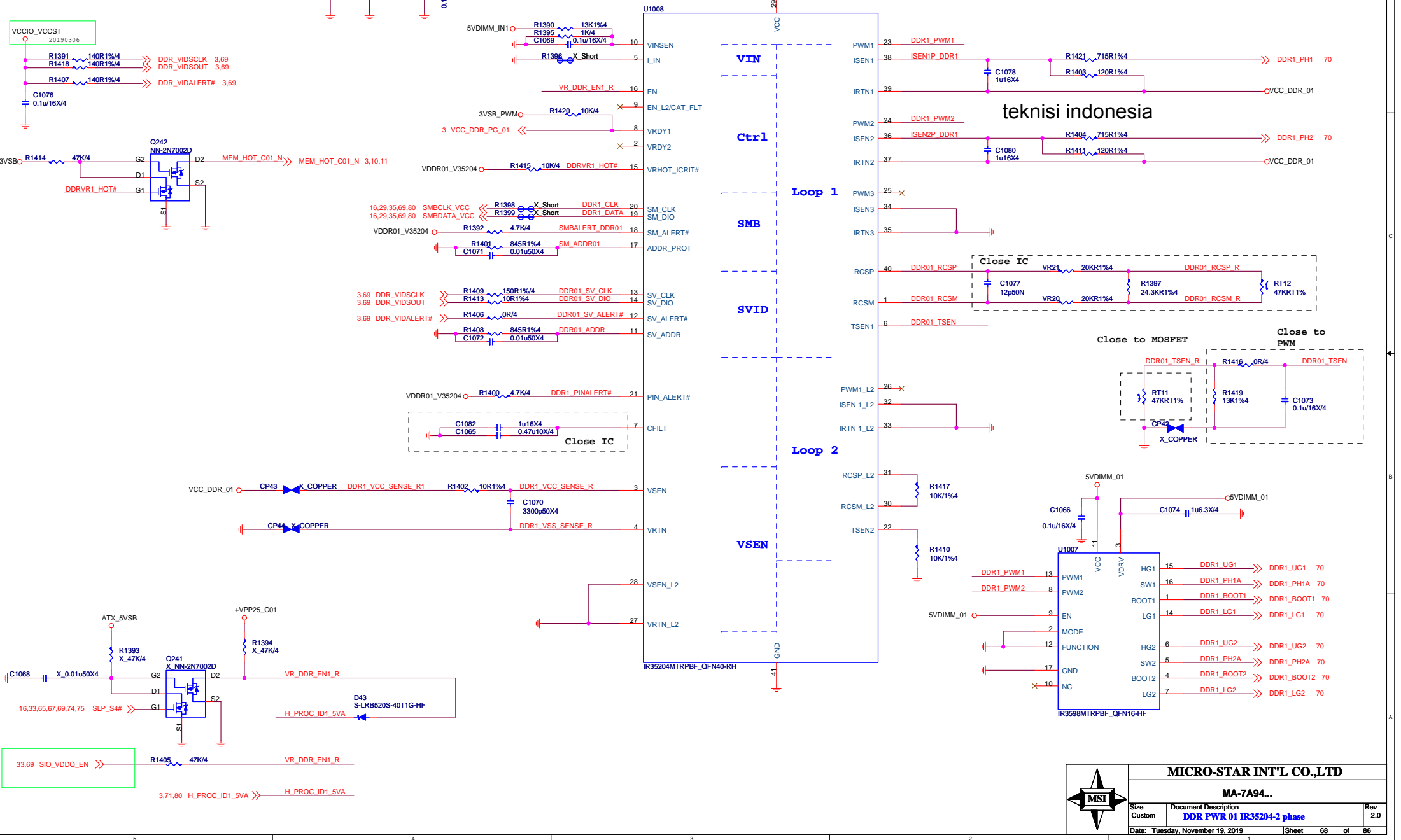
MA-7A94...

Size	Document Description	Rev
Custom	VR13_VSA/VCCIO IR35204	2.0

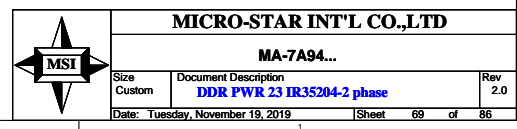
Date: Tuesday, November 19, 2019 | Sheet 65 of 86

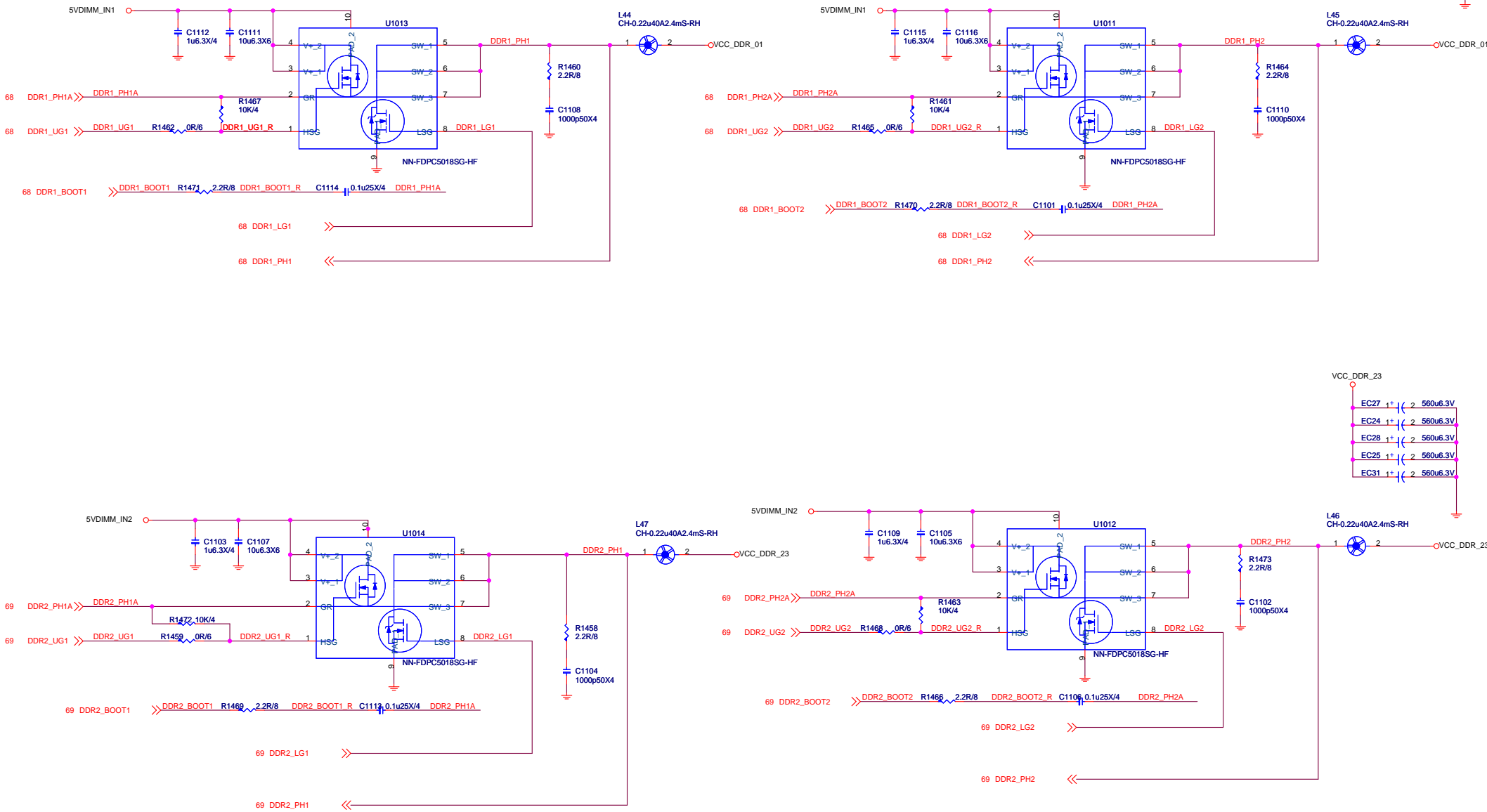


DDR Power1-IR35204-2-Phase
DDR4 1.2V
nominal,
0.8V-2.5V
Max ,39.14A /
OCP 50A



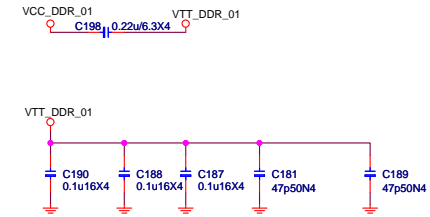
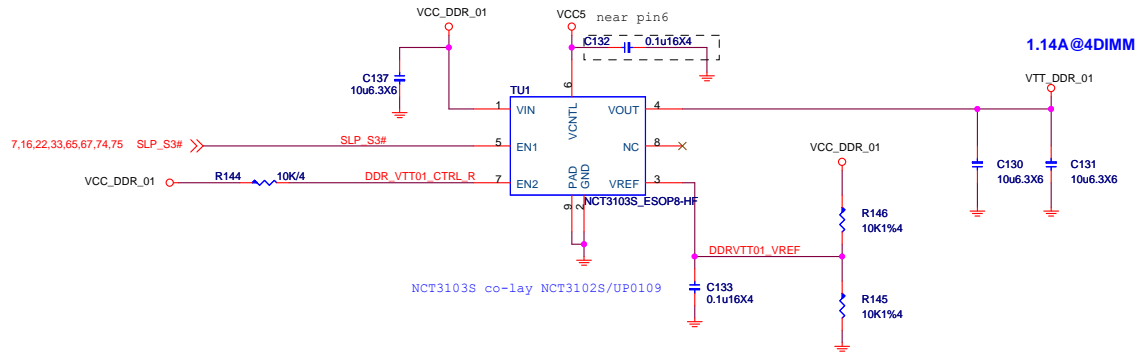
DDR4 1.2V
nominal,
0.8V-2.5V
Max ,39.14A /
OCP 50A





DDR VTT Power

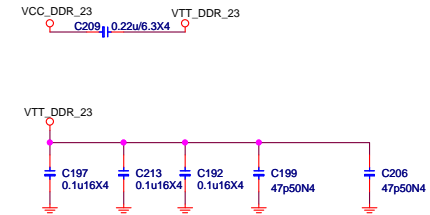
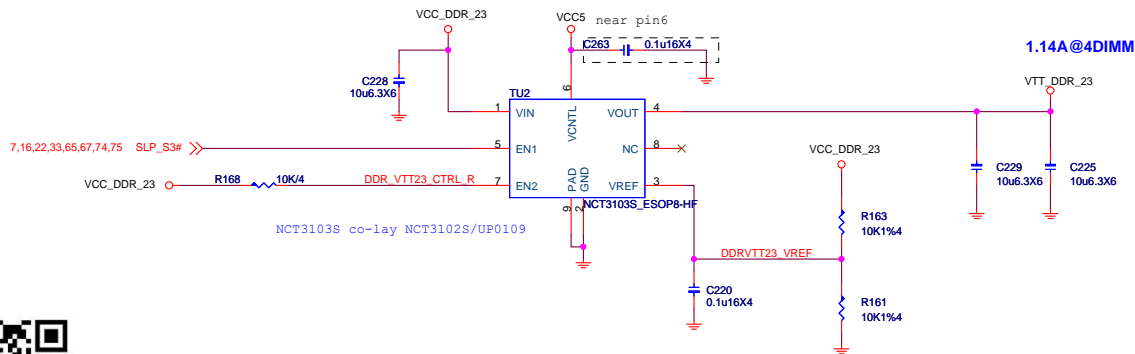
To CPU Copper trace width > 250mils , Fill
island behind DIMM > 400mils .



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DDR VTT Power

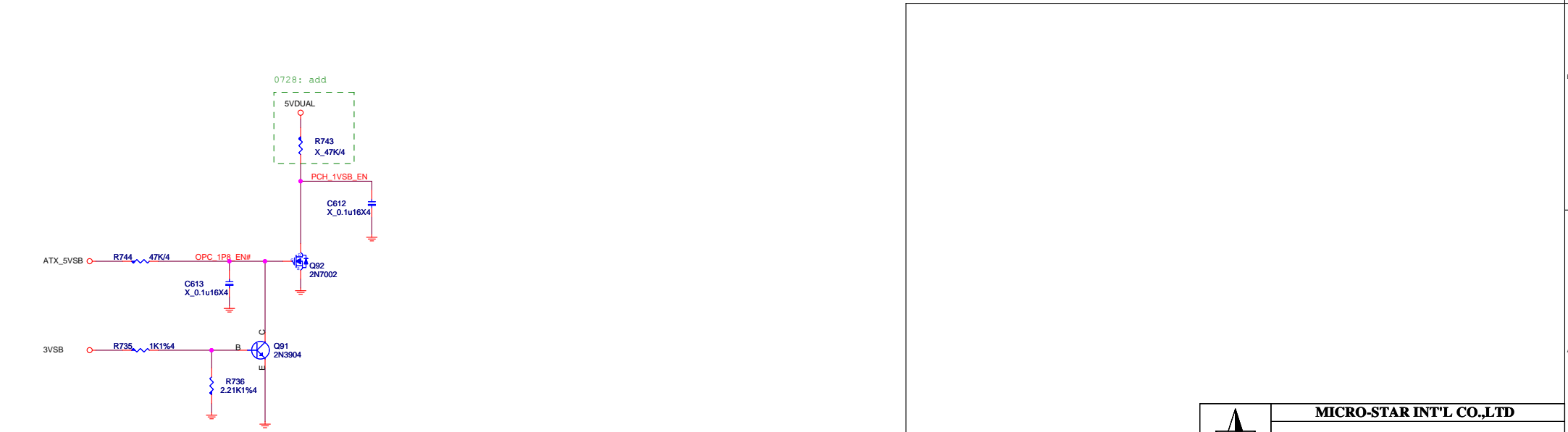
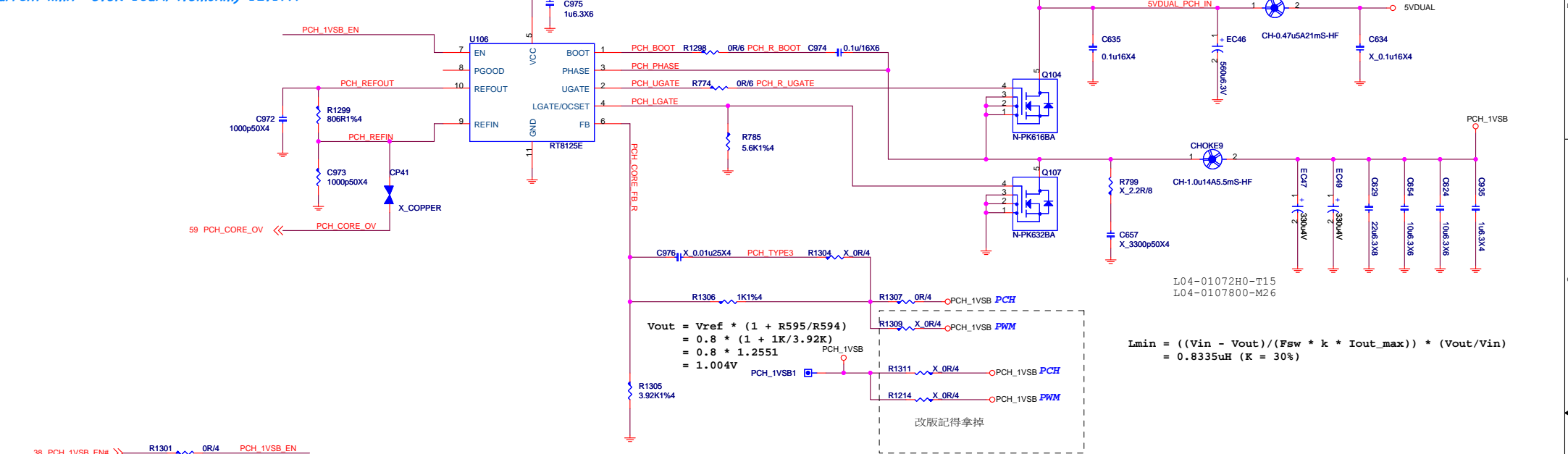
To CPU Copper trace width > 250mils , Fill
island behind DIMM > 400mils .



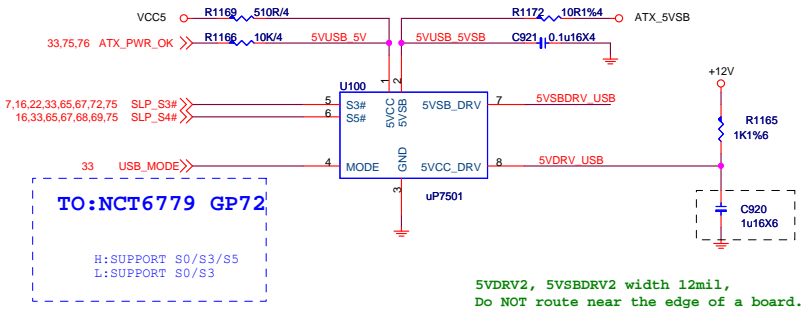
PCH_1VSB Power:1.0V,10A

OCP = 13A R785=5.6K

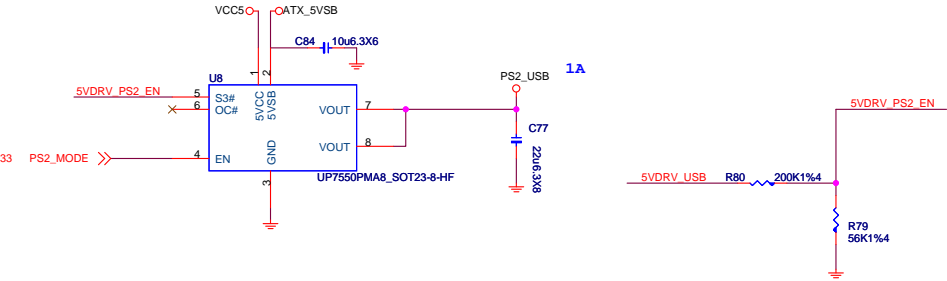
D03-632BA0C-N03
Current limit= 5.6K*10uA/3mohm)=18.66A
Current limit= 5.6K*10uA/4.6mohm)=12.17A



USB POWER

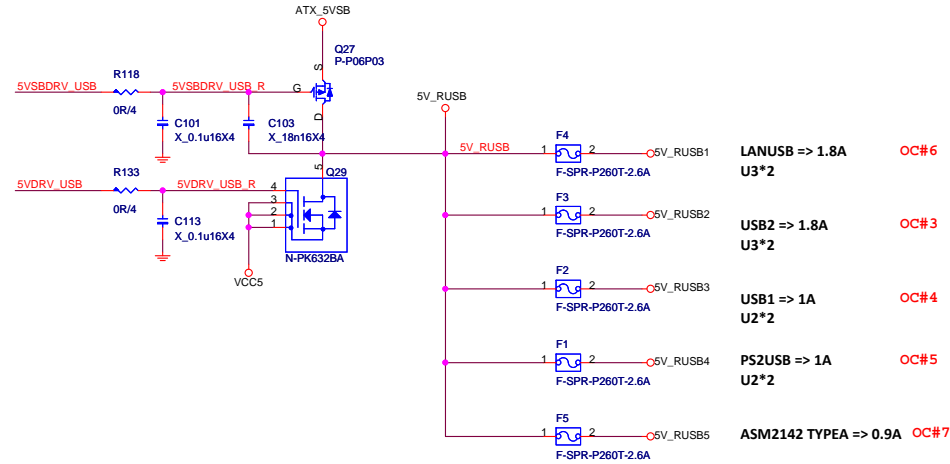


PS2 POWER

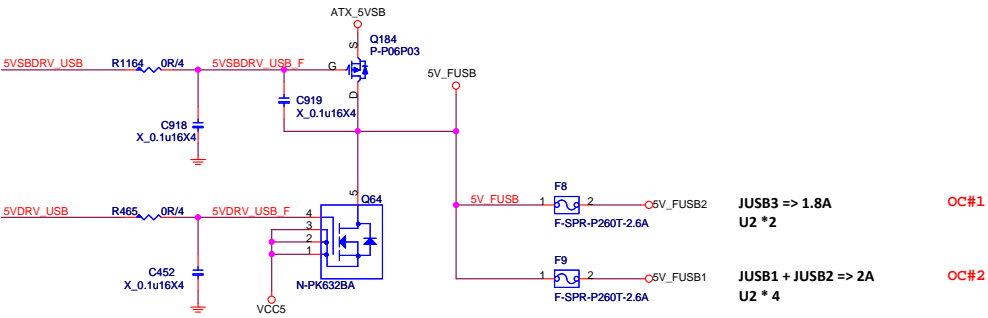


USB MODE

REAR USB PORT POWER

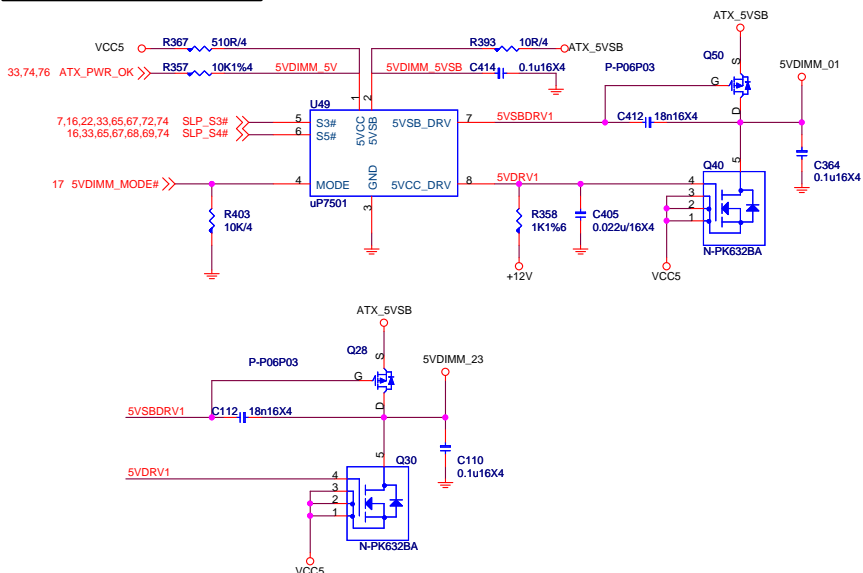


FRONT USB PORT POWER



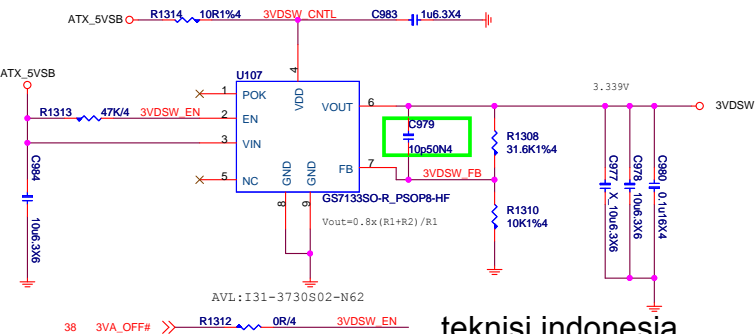
MICRO-STAR INT'L CO.,LTD		
MA-7A94...		
Size Custom	Document Description USB Power	Rev 2.0
Date: Tuesday, November 19, 2019		Sheet 74 of 86

5VDIMM FOR DDR

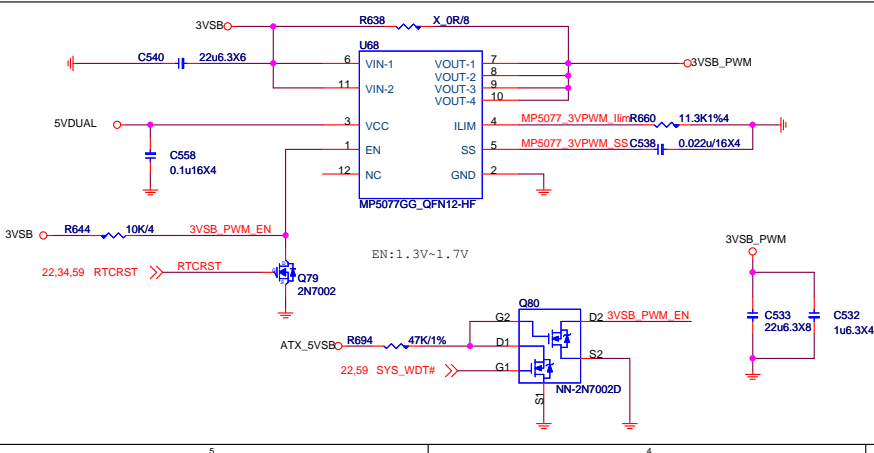


3VDSW

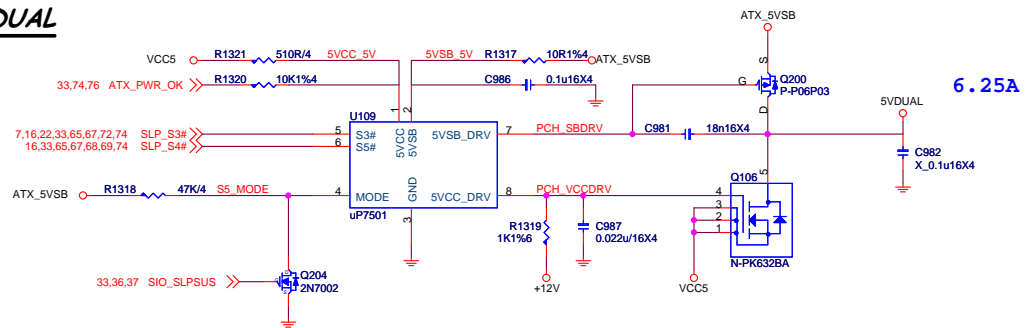
PCH 0.2A+I219 0.15=0.35A



teknisi indonesia

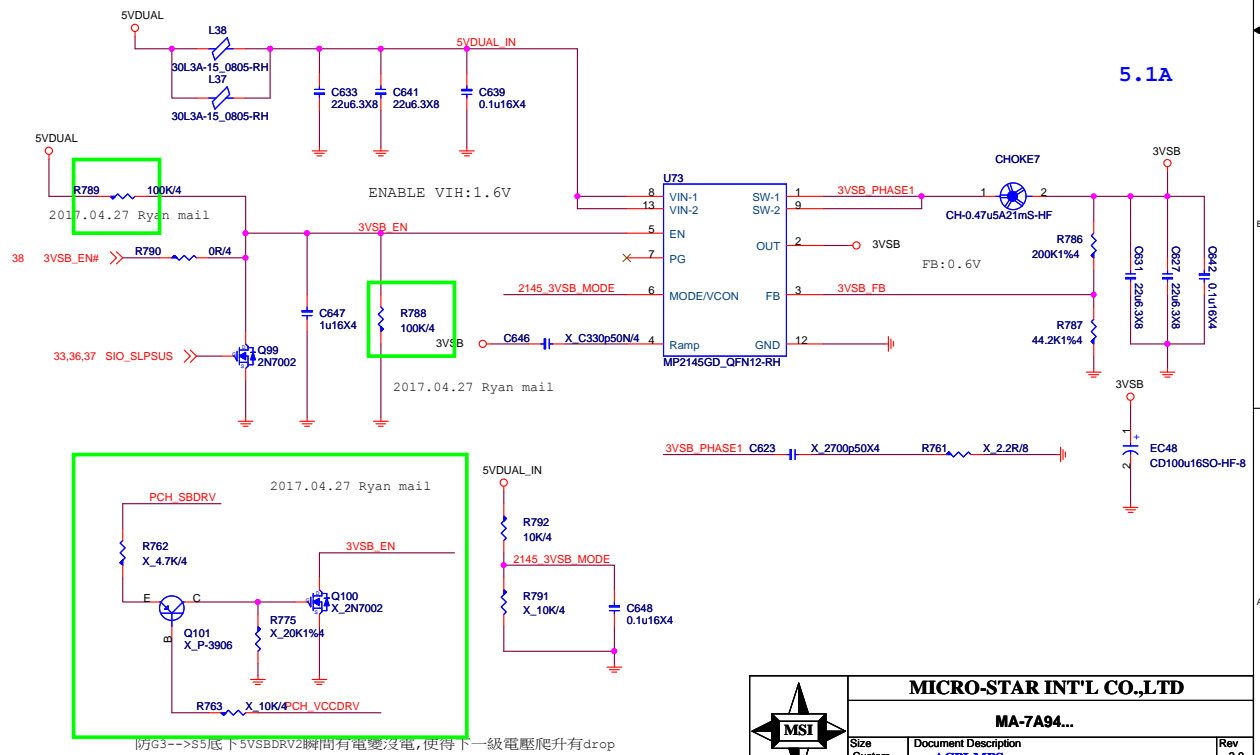


5VDUAL



3VSB

for OC & Gaming



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop



MICRO-STAR INT'L CO.,LTD

MA-7A94...

Size	Custom
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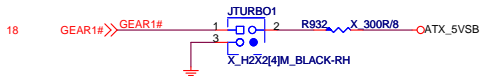
	Document Description
	ACPI-MPS

Rev	
2.0	

Date: Tuesday, November 19, 2019

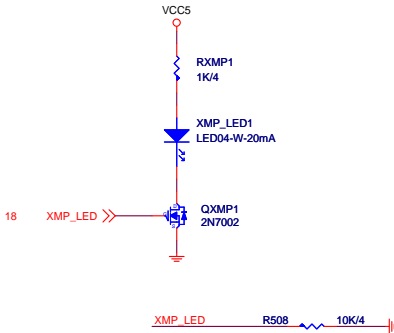
Sheet 75 of 86

JTURBO

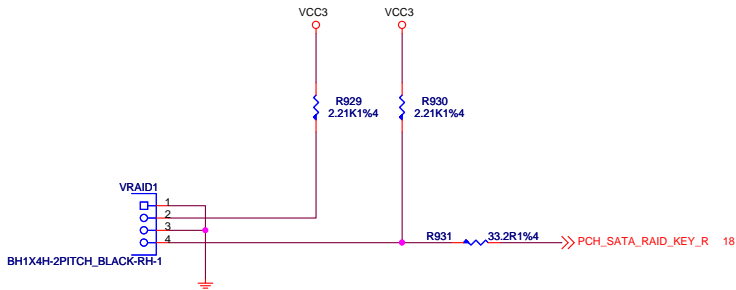


XMP LED

XMP LED >> (default) :D0C-040T200-H91

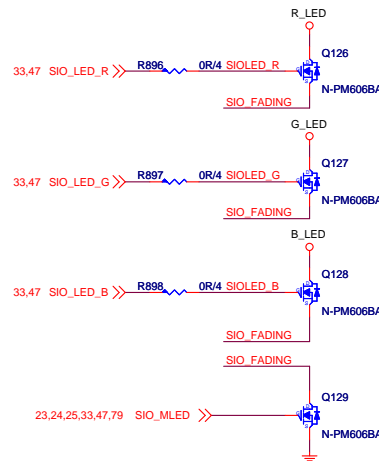
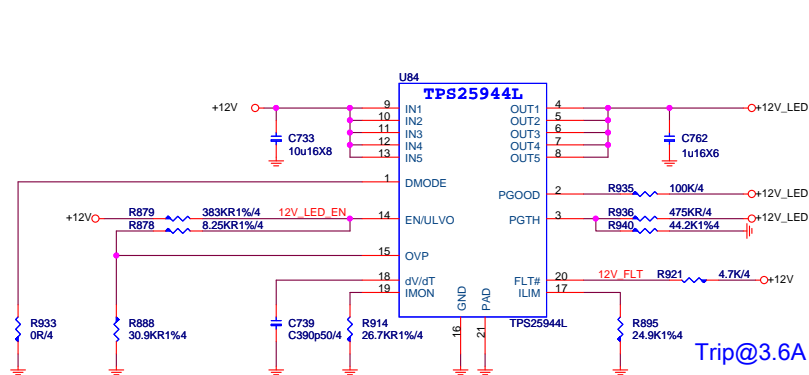


VROC

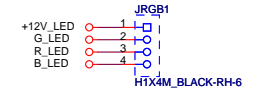
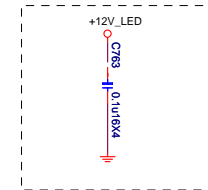


MICRO-STAR INT'L CO.,LTD		
MA-7A94...		
Size Custom	Document Description Turbo/XMP LED/VROC	Rev 2.0
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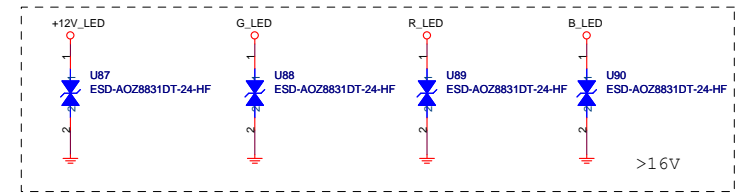
LED STRIPLINE



2016.08.02 Add +12V_LED 0.1uF



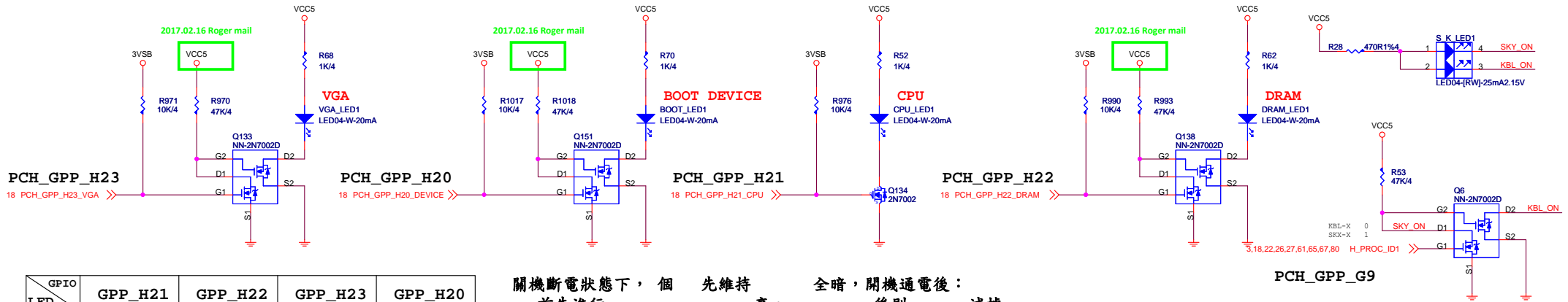
2016.07.06 only reserve now
2016.08.02 stuff BSD



EZ Debug

LED
白 : D0C-040T200-H91
AVL: D0C-040S200-E07

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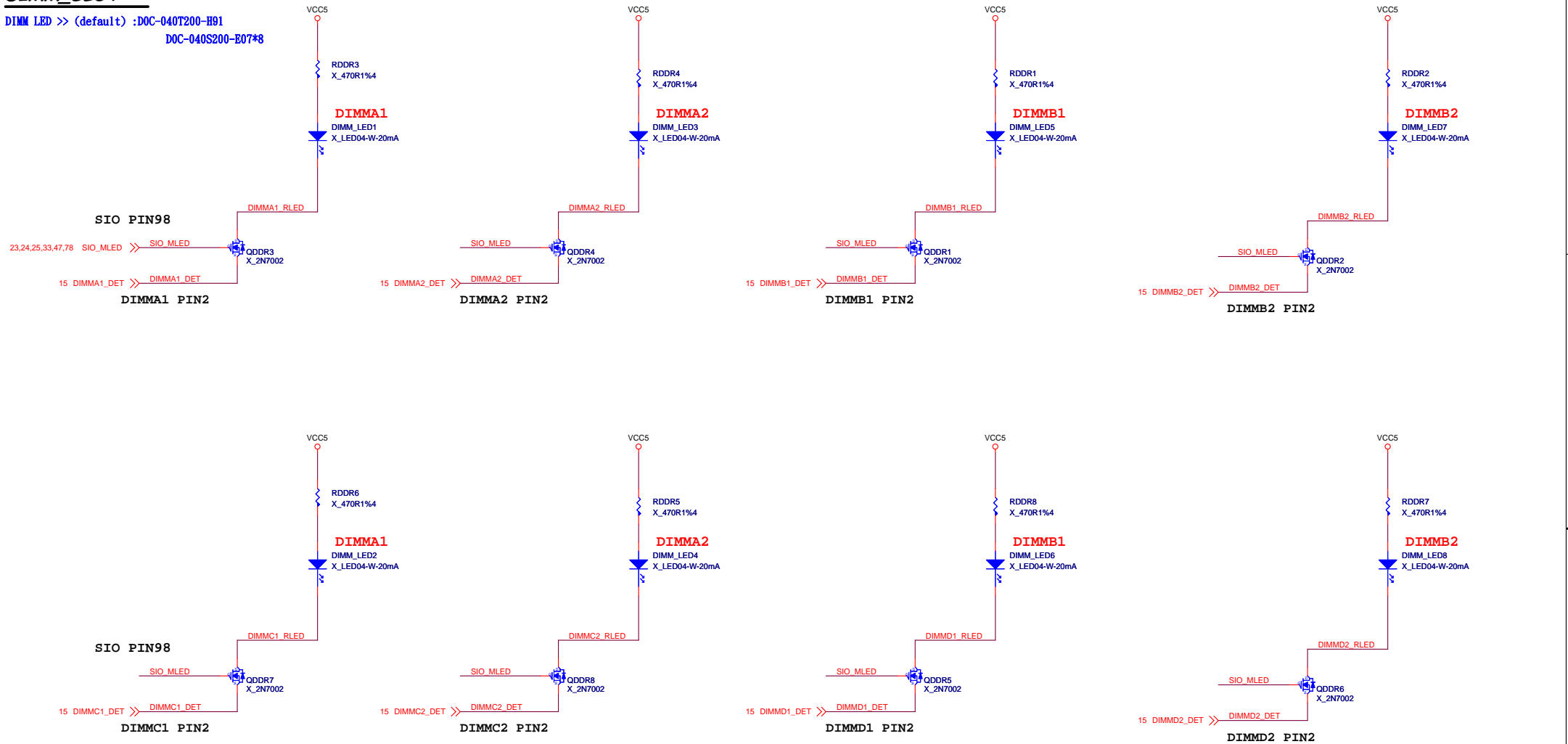


GPIO LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

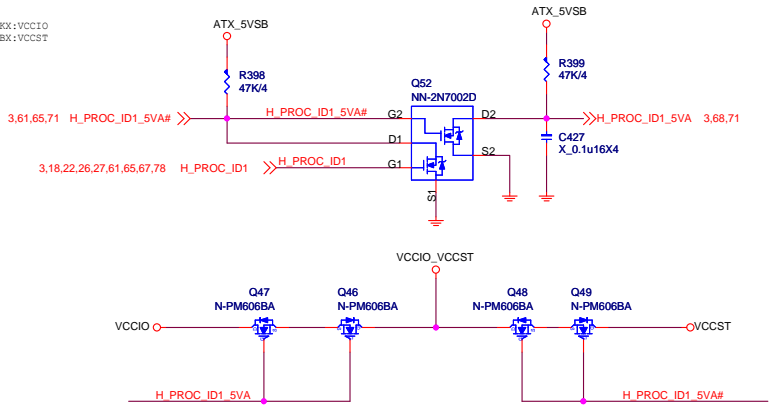
關機斷電狀態下，個 先維持 全暗，開機通電後：
首先進行 亮， 後則 滅掉。
接著依序進行 亮， 後則 滅掉。
的 亮， 後則 滅掉。
的 亮， 後則 滅掉。
因此最後正常順利開機後，四個 燈都是滅掉的。
(系統重啟或其他原因造成系統重開機，則 仍按上述行為動作)

DIMM_SLOT

DIMM LED >> (default) :DOC-040T200-H91
DOC-040S200-E07*8

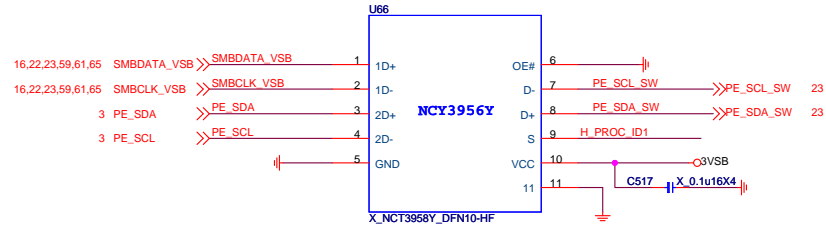


SKX:VCCIO
KBX:VCCST

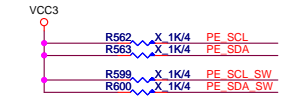


PEG_PCIE_SLOT SMBUS SWITCH

SKX: PEG
KBX: PCH

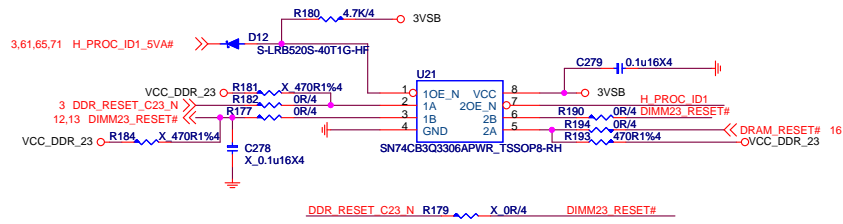


OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D



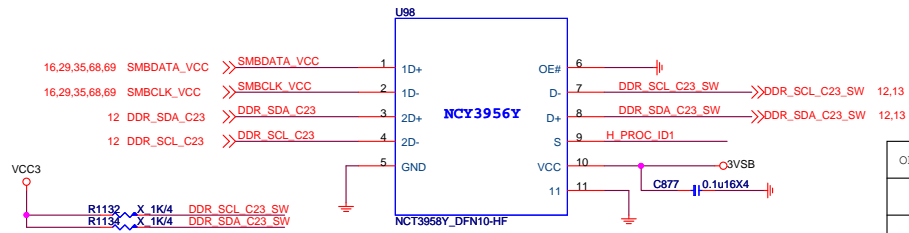
DDR23_RESET SWITCH

SKX: PEG
KBX: PCH



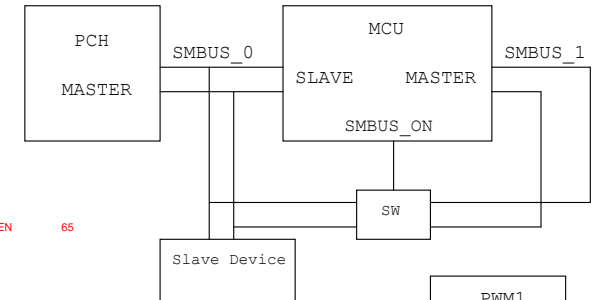
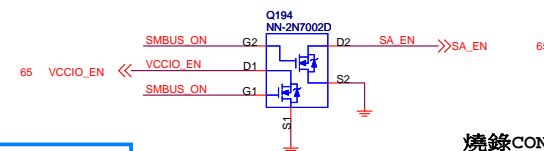
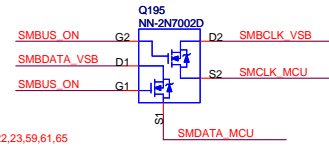
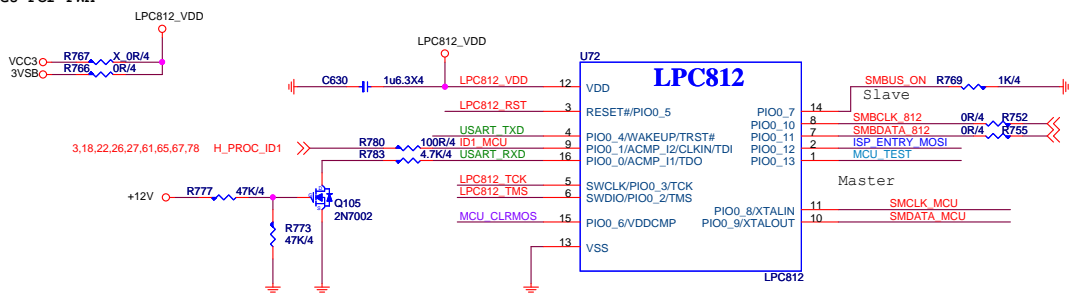
DIMM_SLOT SMBUS SWITCH

SKX: PEG
KBX: PCH

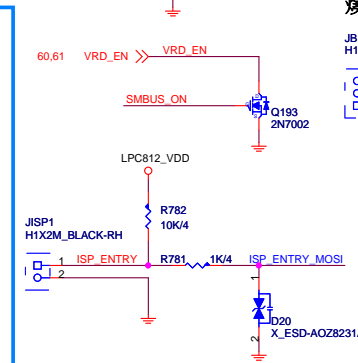
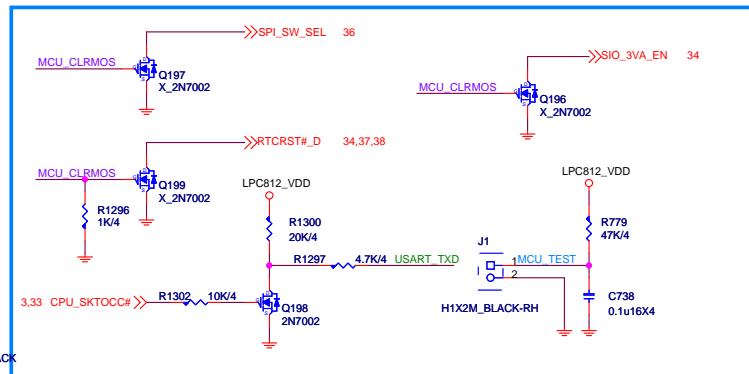
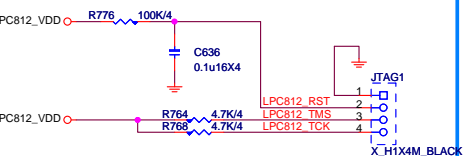


OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

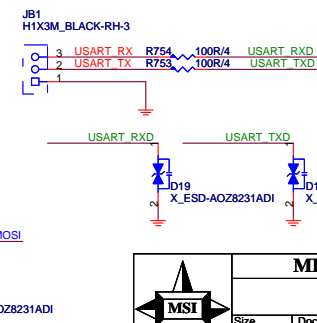
MCU For PWM



JTAG for SW DEBUG



燒錄CONNECT



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MA-7A94...		
Size	Document Description	Rev
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HEATSINK

CPU_H1
CPU
鐵座
CPU_ILM1
2017.05.22 PM Change

PCB1
7A94_10
PD0-07A9410-G37
PD0-07A9410-E48

VIRTUAL1
Label
VIRTUAL
X_VIRTUAL

BAT1_X1
BAT-BCR2032P-RH

COVER1
CHOKER
Cover
X1
X2
X_COVER

BIOS_LA1
AMI_BIOS
LABEL
G51-M1SPXXA-A09

LABE5
SLI
LABEL
Y01-RNVIDIM-000

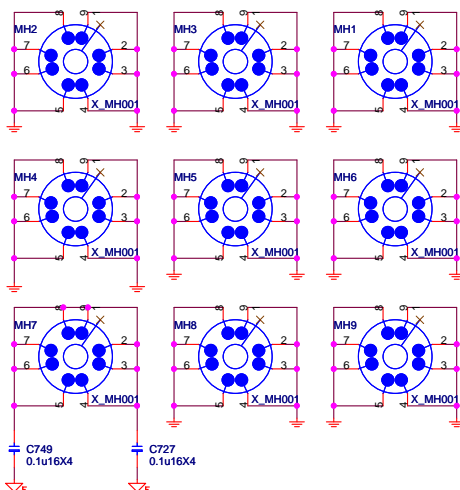
MKT_LA1
MKT LABEL
G51-M1SPL38-Q13

MKT_LA2
MKT LABEL
X_G51-M1SPL38-Q13

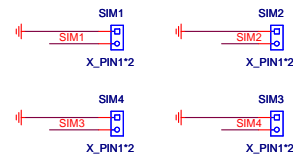
MOS_SINK1
MOS
SINK
MOS_SINK1
MCE1
MCE2

PCH_SINK1
MEC1
MEC2
MEC3
MEC4
PCH_SINK1

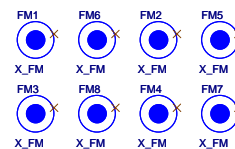
Mounting Holes



Simulation



Optical Fiducial Marks-120



Test point

